INSTANT CONTROLLED SWITCHING OF TRANSFORMERS

DISSERTATION SUBMITTED
IN PARTIAL FULFILMENT OF THE REQUIREMENTS
FOR THE AWARD OF THE DEGREE OF

MASTER OF SCIENCE
IN
ELECTRICAL ENGINEERING
(SYSTEMS ENGINEERING)

BY

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C E R T I F I C A T E

Certified that the dissertation entitled,'Instant Controlled Switching of Transformers', which is being submitted by Mr. Ateeq Ahmad in partial fulfilment of requirements for the award of the degree of Master of Science in Electrical Engineering (System Engineering) of the Aligarh Muslim University, Aligarh, is a record of the candidate's own work carried out by him under our supervision and guidance. The matter embodied in this dissertation has not been submitted for the award of any other degree or diploma.

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DISSERTATION APPROVAL SHEET

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SYNOPSIS

This dissertation deals with the problem of switching transients in a transformer. The inrush has been theoretically estimated taking into account the saturation in the magnetic circuit for various values of the switching instant.

An electronic circuit is then designed and fabricated to control the switching instant. As a matter of fact the major portion of this work is composed of the details of this circuit.

The test results making use of the circuit are then practically obtained and compared with theoretical results.

C O N T E N T S

CHAPTER -1

INTRODUCTION

INTRODUCTION

Initial transient current in an AC electrical circuit depends primarily on the instant at which voltage is applied besides voltage magnitude and initial conditions[1]. In all power system equipments, voltage level is selected mainly from the point of view of economy and practicability at the design stage and hence can not be changed once selected[2]. To control the initial conditions in most of the equipments are difficult and even impossible in some cases. More-over by controlling these two factors (i.e. voltage magnitude and initial conditions) initial transient current can only be reduced to a low level but can not be eliminated altogether. However by controlling the instant of application of voltage it can be reduced substantially and can even be eliminated in most of the cases[3].

The problem of switching transients in a transformer is specially taken up for this dissertation. The problem is analytically dealt with in Chapter-2. Subsequently in Chapter-3 a controlled instant switching scheme is formu-

lated. Digital ICs and few descrete components are used in realization of the scheme. The use of ICs makes the circuit compact and reliable. Commercially available ICs of 74 series are used in realization of the scheme. A complete theory and outline along with the block diagram of the proposed scheme is discussed in Chapter-3. A systematic design of each bulding block of the proposed scheme is described in Chapter-4. Testing procedures both manual as well as automatic, along with experimental results are included in Chapter-5. An extension of the proposed scheme with concluding remarks is suggested in the last Chapter. The design of Power Supplies, ICs pin diagrams, computer program, lay out diagram etc. are enclosed in the appendices.

CHAPTER - 2

THEORETICAL STUDY OF INITIAL INRUSH CURRENT OF A TRANSFORMER

THEORETICAL STUDY OF INITIAL INRUSH CURRENT OF A TRANSFORMER

In this chapter an effort is made to show the nature of initial inrush of magnetizing current and its dependence on switching instant. It is seen that if the switching instant is controlled then the inrush current can be substantially reduced.

2.1. Theoretical Study

When the primary side of a transformer is switched-on to normal voltage with secondary side open circuited, it acts exactly like a simple inductive reactor. At every instant the voltage applied must be balanced by the e.m.f induced by the flux generated in the core plus the small drops in the resistance and leakage reactance. This flux is generated by the magnetizing current. To understand the nature of inrush current qualitatively let us assume that only the induced e.m.f balances the applied voltage and the drops across resistance and leakage reactance are negligible.

Let us also assume that the core is initially demagnetized and the switch closes at the peak of the voltage. The e.m.f must be established spontaneously. This demands a maximum rate of change of flux. The maximum rate of change in the flux occurs at the zero crossing instants when it changes its polarity (direction) from negative to positive or vice versa and so does the magnetizing current. These conditions which obtain immediately after the closing of the switch, are however precisely the same as the final steady conditions so that the energization of the transformer proceeds without any transients. Thus when the transformer is switched-on at the instant when the applied voltage passes through peak value, the voltage, the flux and e.m.f wave immediately assume the steady conditions as shown in Fig.-2.1(a).

Assume now that the switch closes at the instant when the applied voltage passes through a zero value and increasing in the positive direction. Throughout the first half cycle, the voltage is positive and

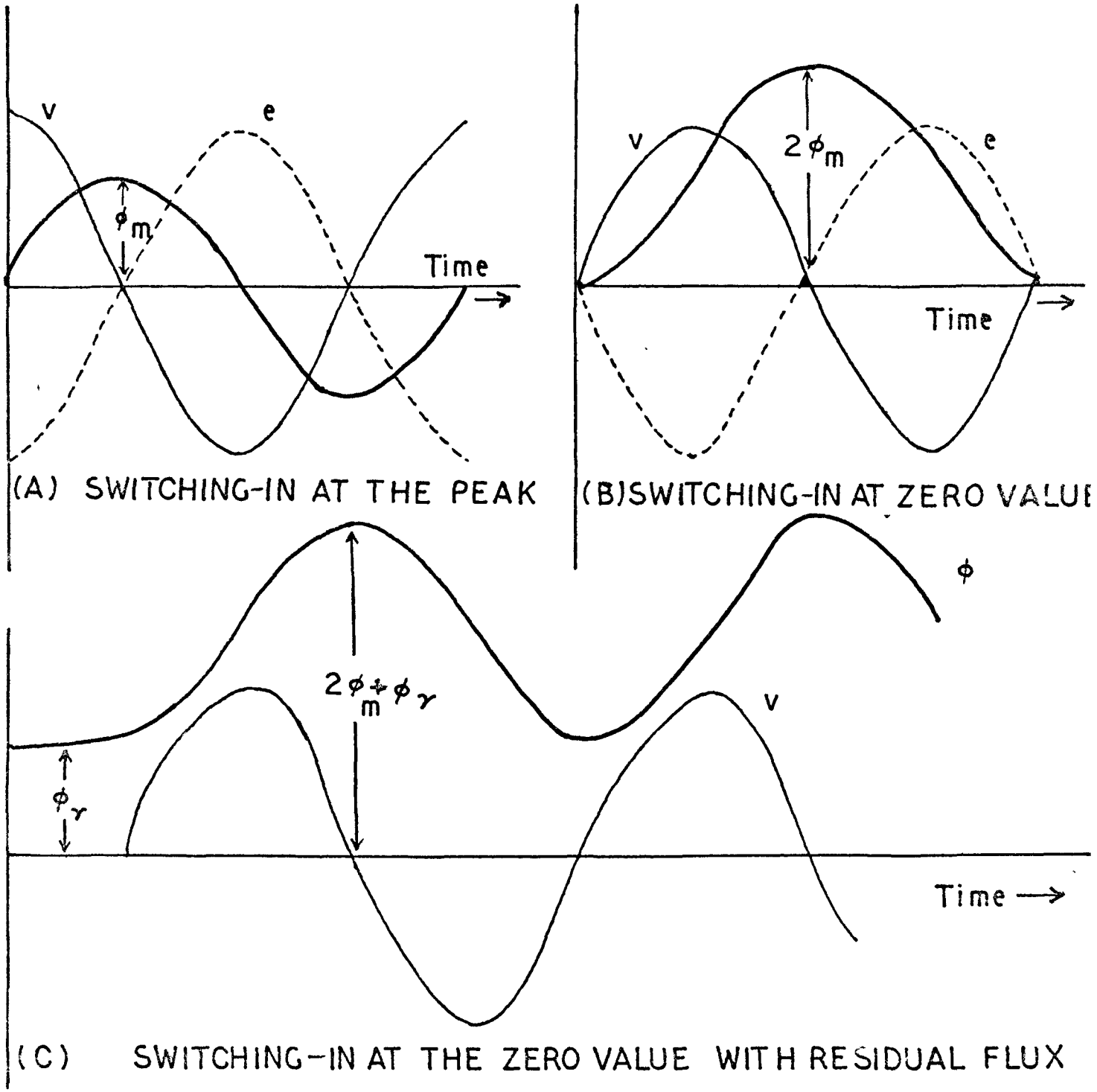


FIG. 2.1 SWITCHING-IN TRANSIENTS IN A TRANSFORMER

consequently the e.m.f is negative (i.e. in phase opposition). The flux for this half period therefore must continuously increases. It begins at zero value with an increasing rate of change and finally reaches about double of its normal peak value at the end of the first half cycle. This effect is known as doubling effect. This is shown in Fig.-2.1(b).

The modern trend of design is that under normal working conditions the transformer is scheduled to operate almost at the knee point of the magnetization curve. This is desired in order to reduce the dead weight of the transformer and have more economical design. Any increase in flux and therefore the flux density pushes the transformer into the saturation region of the magnetization curve. Consequently the required percentage increase in the magnetization current will be much more than the corresponding percentage increase in the flux or flux density. The doubling effect of flux, discussed above may demand a magnetizing current very many times the normal rated

current of the transformer although the usual value of this current is only a small percentage of the rated current.

Upto now two extreme cases are explained (i) when the switch is closed at the peak of applied voltage which causes no transients (ii) when the switch is closed at zero cross-over instant of the applied voltage and very high magnetizing currents are resulted. In practical cases the switch may be closed-on at any voltage magnitude between peak value and zero value and the severity of magnetizing current depends on the corresponding instant.

The presence of the residual magnetism in the core may further increase the inrush current. If the voltage is switched-on at a zero instant in such a way that initial flux produced has the same direction as the residual flux ϕ_r, the resultant wave form of the flux will be as shown in Fig.-2.1(c). The flux wave offsets by an amount ϕ_r and now the peak value of flux becomes $2\phi_m + \phi_r$.

2.2. Analytical Study

For analytical study a simple equivalent circuit of a transformer is choosen.

Here R_1 is the primary resistance including internal resistance of the supply.

R_2, L_2 are secondary resistance and inductance including the load.

n_1, n_2 are the number of turns of primary and secondary windings respectively.

i_1, i_2 are primary and secondary currents.

i_m is magnetizing current.

Let the applied voltage be given by

$$e = Em \sin(\omega t + \partial)$$

where ∂ decides the instantaneous value of e when the switch is closed at t = 0.

The following equations can easily be written for this circuit.

$$Em\ Sin(\omega t + \delta) = R_1 i_1 + n_1 \frac{d\phi}{dt} \qquad (1)$$

$$n_2 \frac{d\phi}{dt} = L_2 \frac{di_2}{dt} + R_2 i_2 \qquad (2)$$

$$i_1 = i_m + \frac{n_2}{n_1} i_2 \qquad (3)$$

$$i_m = f(\phi) \qquad (4)$$

These equations can be rewritten by considering small physical changes in the quantities involved, as

$$\Delta\phi = EmSin(\omega t + \delta) \frac{\Delta t}{n_1} - R_1 i_1 \frac{\Delta t}{n_1} \qquad 1(a)$$

$$\Delta i_2 = \frac{n_2 \Delta\phi - R_2 i_2 \Delta t}{L_2} \qquad 2(a)$$

The relation between i_m and ϕ is non-linear. The value of i_m for particular value of ϕ can be determined from magnetization curve as shown in Fig.-2.2. This curve is assumed to be piecewise linear by considering it as consisting of very small segments which are approximated as straight lines.

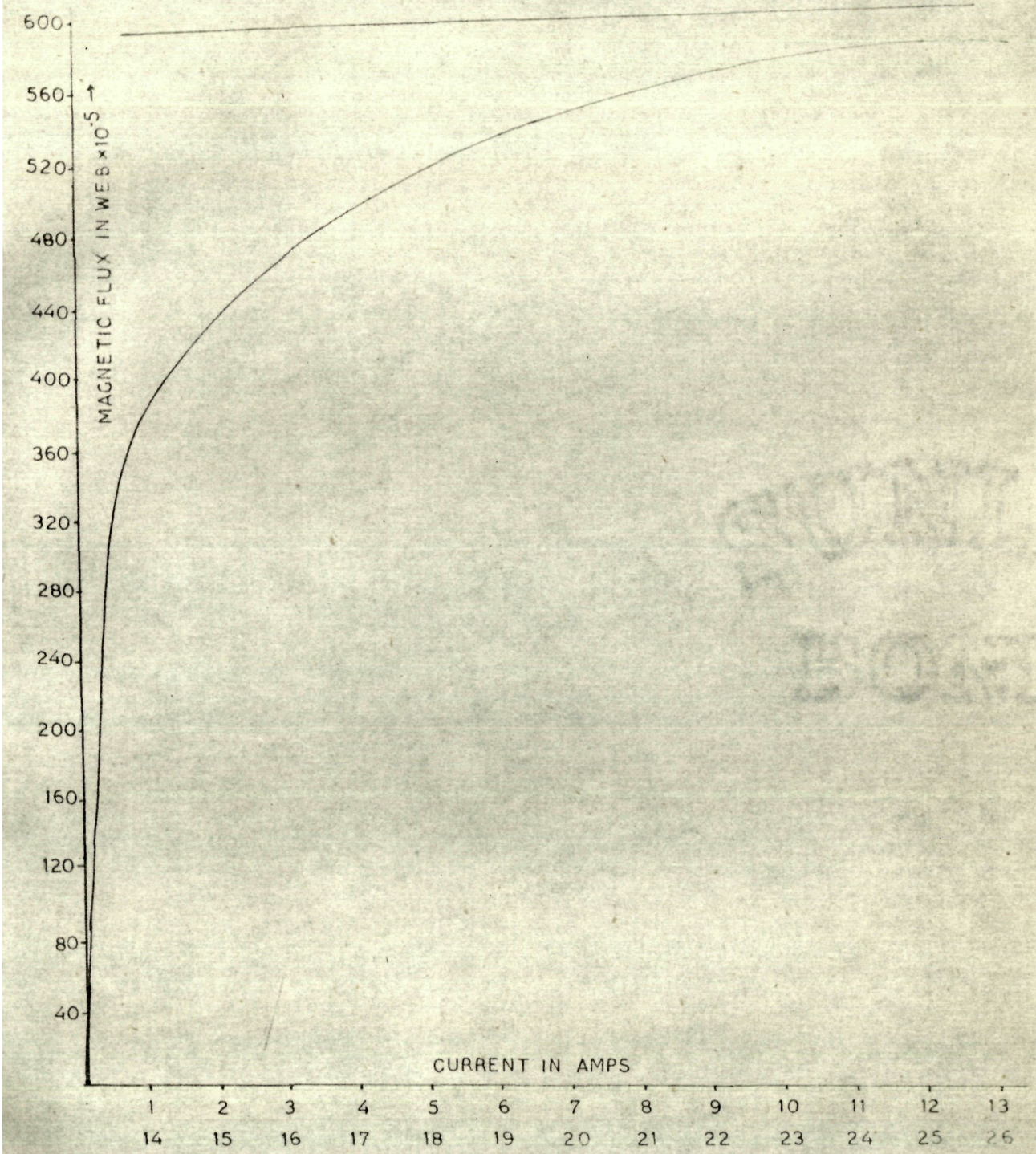


FIG 2.2 MAGNETIC FLUX V/S MAGNETIZING CURRENT

For the computation of the quantities the initial values of ϕ and i_2 are assumed as zero at zero instant (i.e. at t = 0). Now equations (4), (3), 1(a) and 2(a) are used in the given sequence to find the changes in the flux and currents. Next, t is incremented by $\triangle t$ and calculation repeated in the same sequence assuming the values of ϕ and i_2 calculated earlier as initial values. The sequence is repeated upto few cycles.

The numerical values of various parameters are given below :

$\triangle t$ = .0005 Seconds

n_1 = 226

n_2 = 113

R_1 = .365 Ohms

R_2 = 5.24 Ohms

L_2 = .01263 Henery

The results are shown in fig2.3 for various values of ∂ i.e. for various closing instants of the switch. The computer program used is given in Appendix (A).

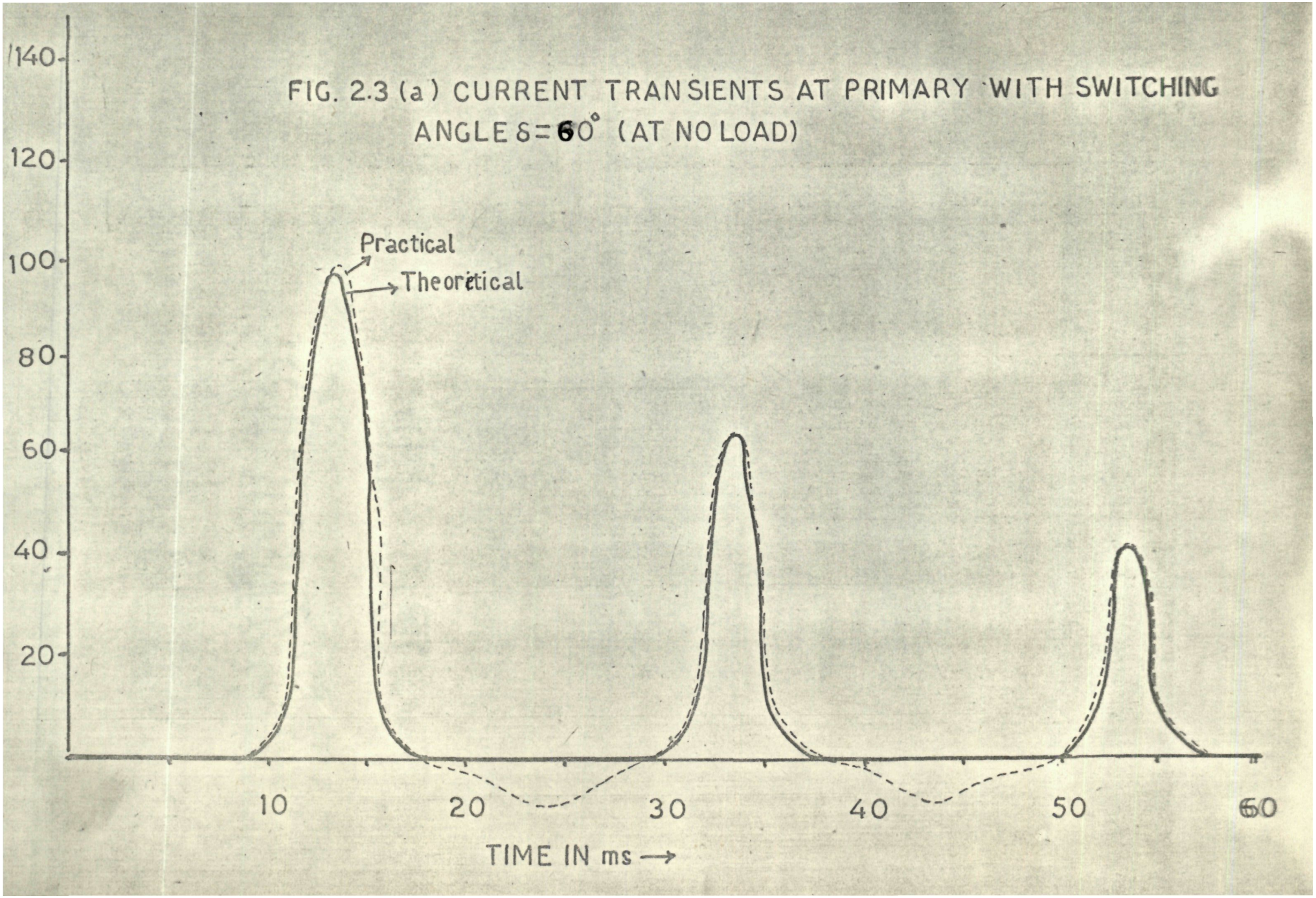


FIG. 2.3 (a) CURRENT TRANSIENTS AT PRIMARY WITH SWITCHING ANGLE $\delta = 60^{\circ}$ (AT NO LOAD)

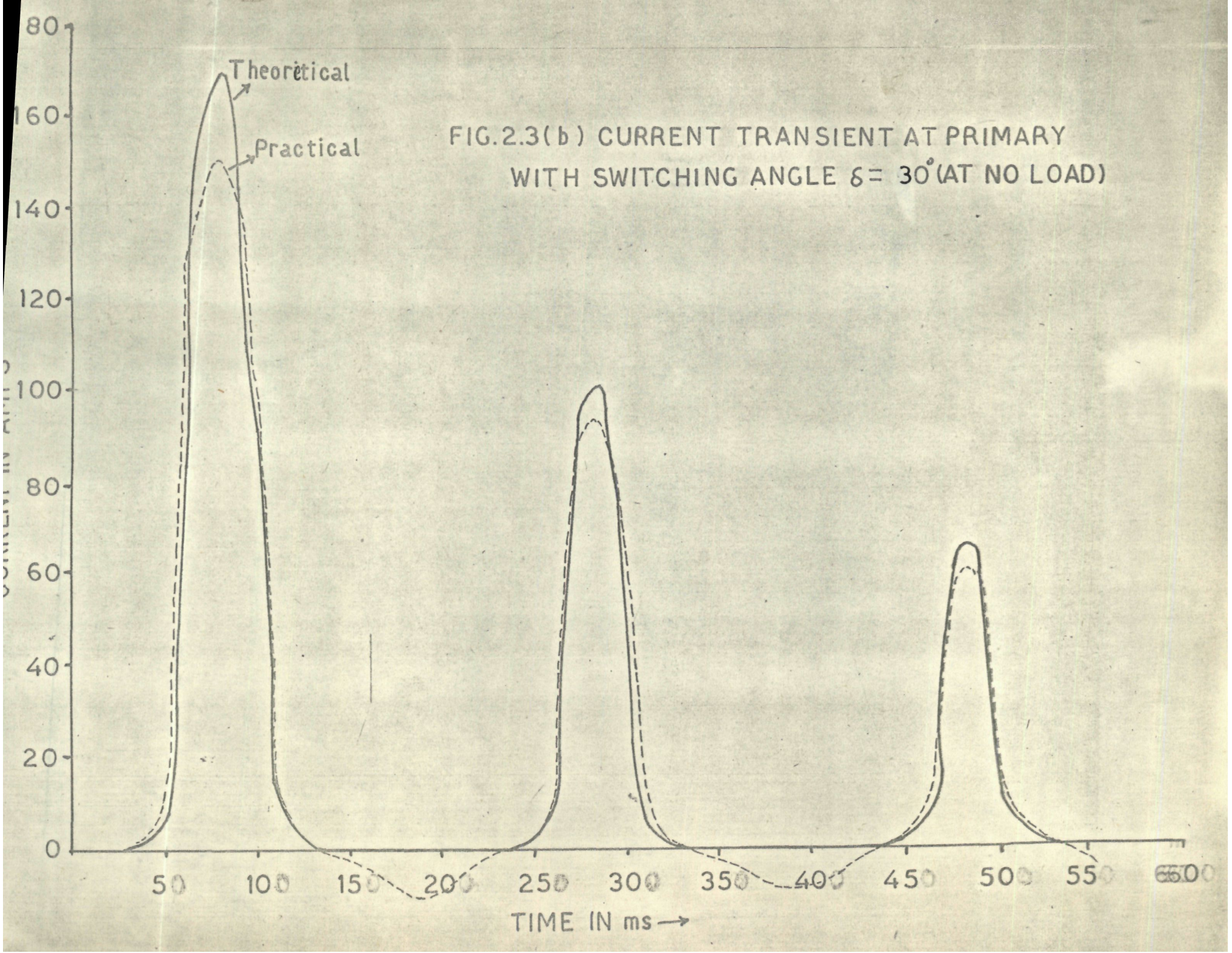


FIG. 2.3(b) CURRENT TRANSIENT AT PRIMARY WITH SWITCHING ANGLE $\delta = 30^{\circ}$ (AT NO LOAD)

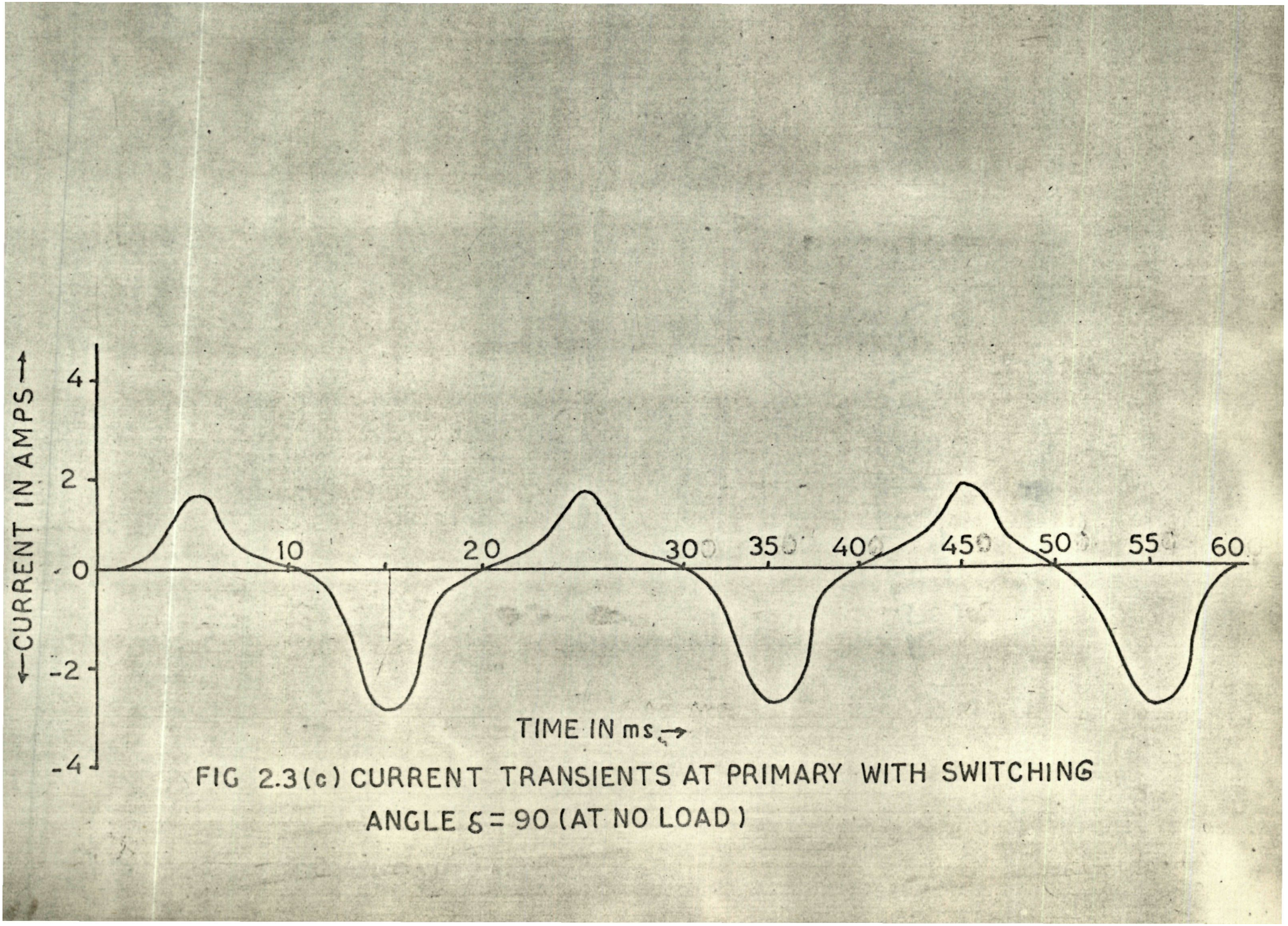


FIG 2.3(c) CURRENT TRANSIENTS AT PRIMARY WITH SWITCHING ANGLE $\delta = 90$ (AT NO LOAD)

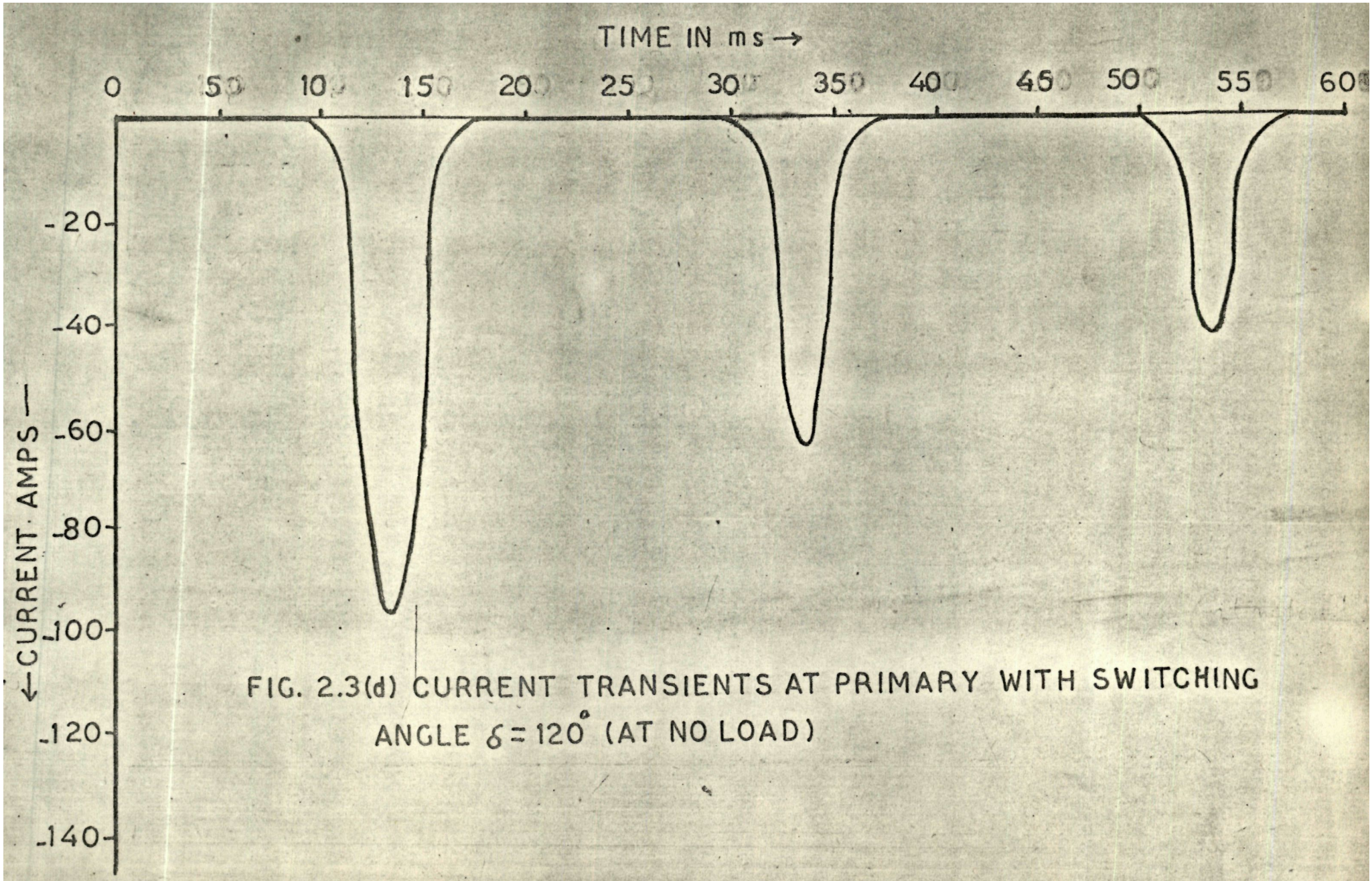


FIG. 2.3(d) CURRENT TRANSIENTS AT PRIMARY WITH SWITCHING ANGLE $\delta = 120^{\circ}$ (AT NO LOAD)

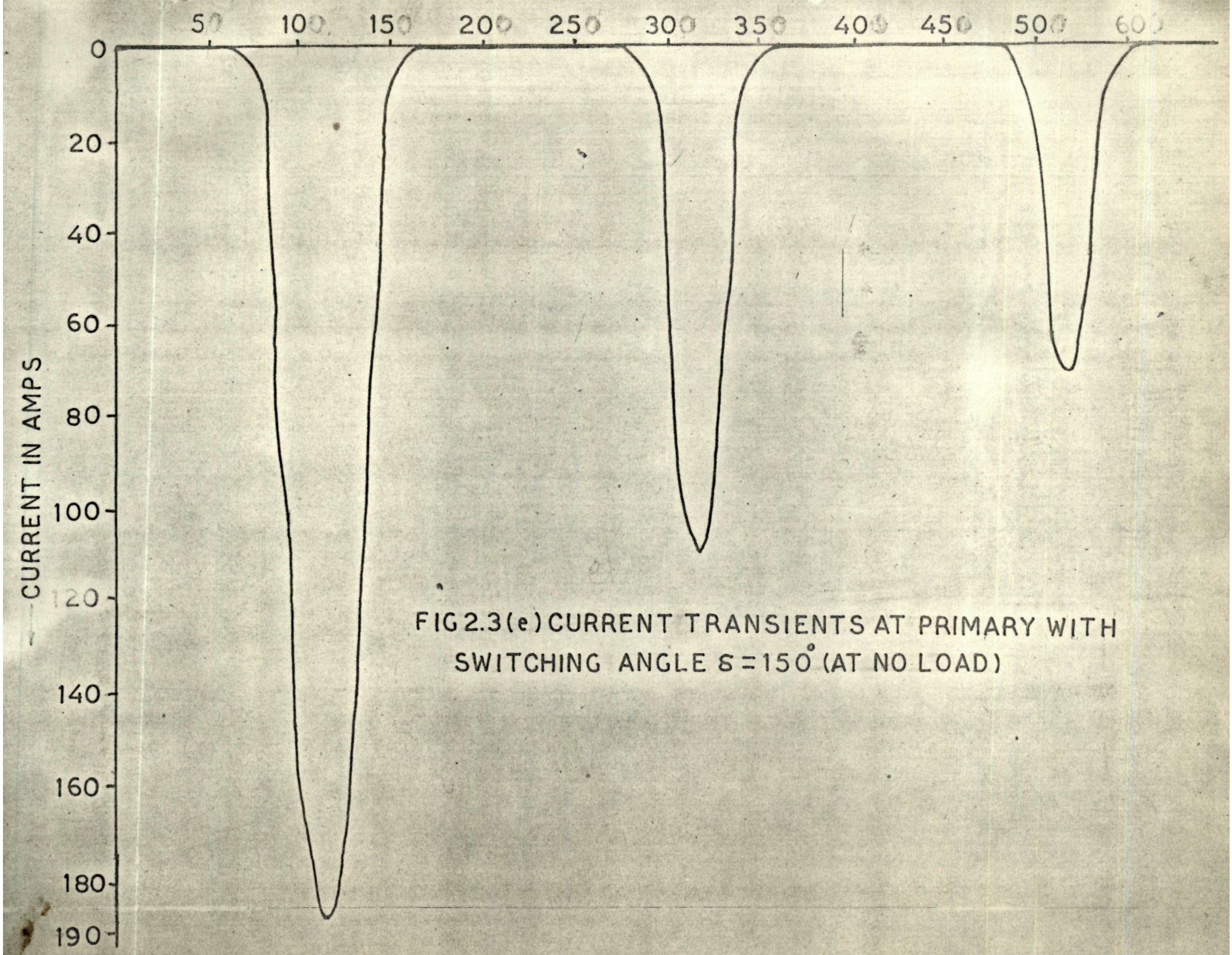


FIG 2.3(e) CURRENT TRANSIENTS AT PRIMARY WITH SWITCHING ANGLE $\delta = 150^{\circ}$ (AT NO LOAD)

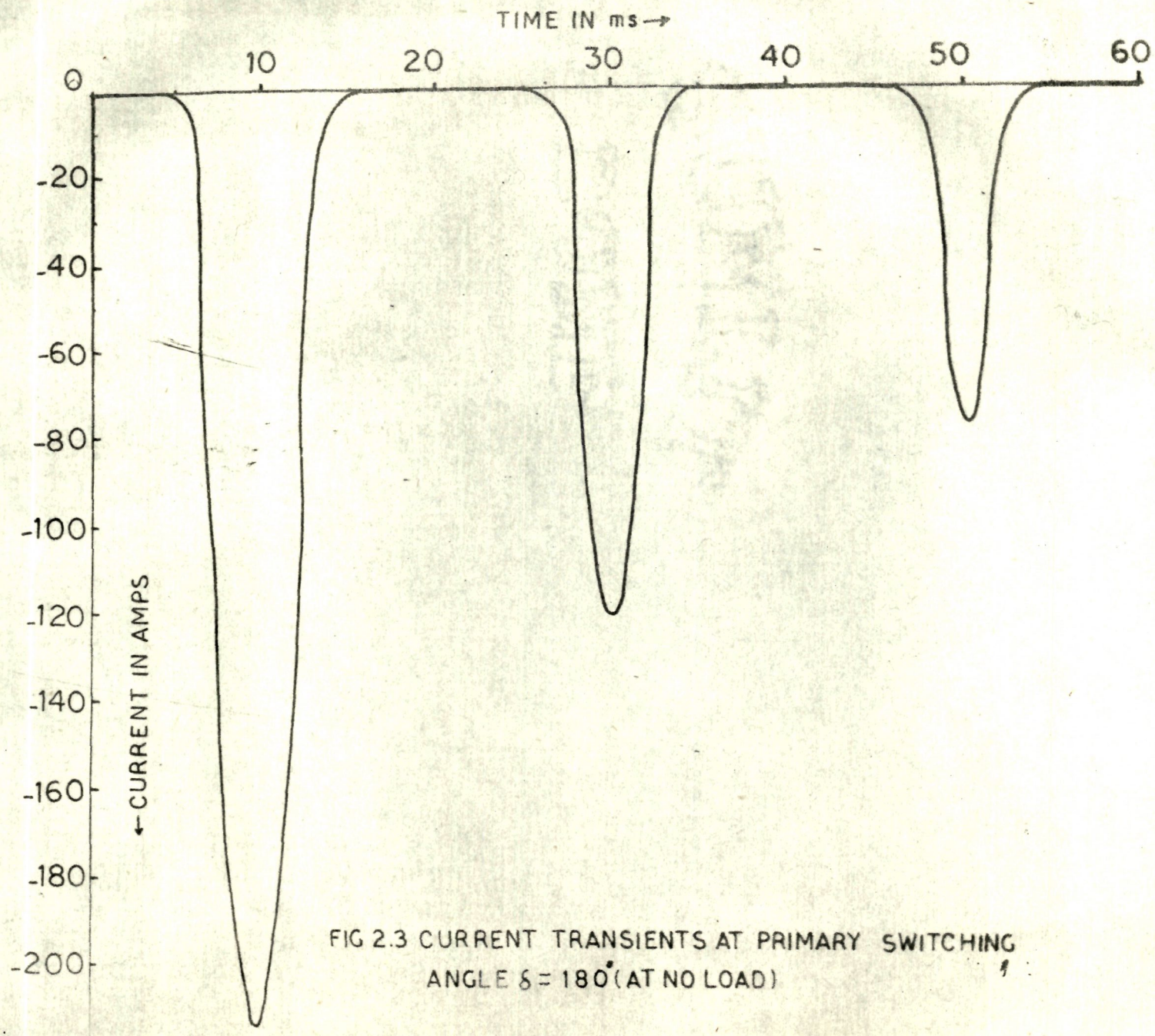


FIG 2.3 CURRENT TRANSIENTS AT PRIMARY SWITCHING ANGLE $\delta = 180^{\circ}$ (AT NO LOAD)

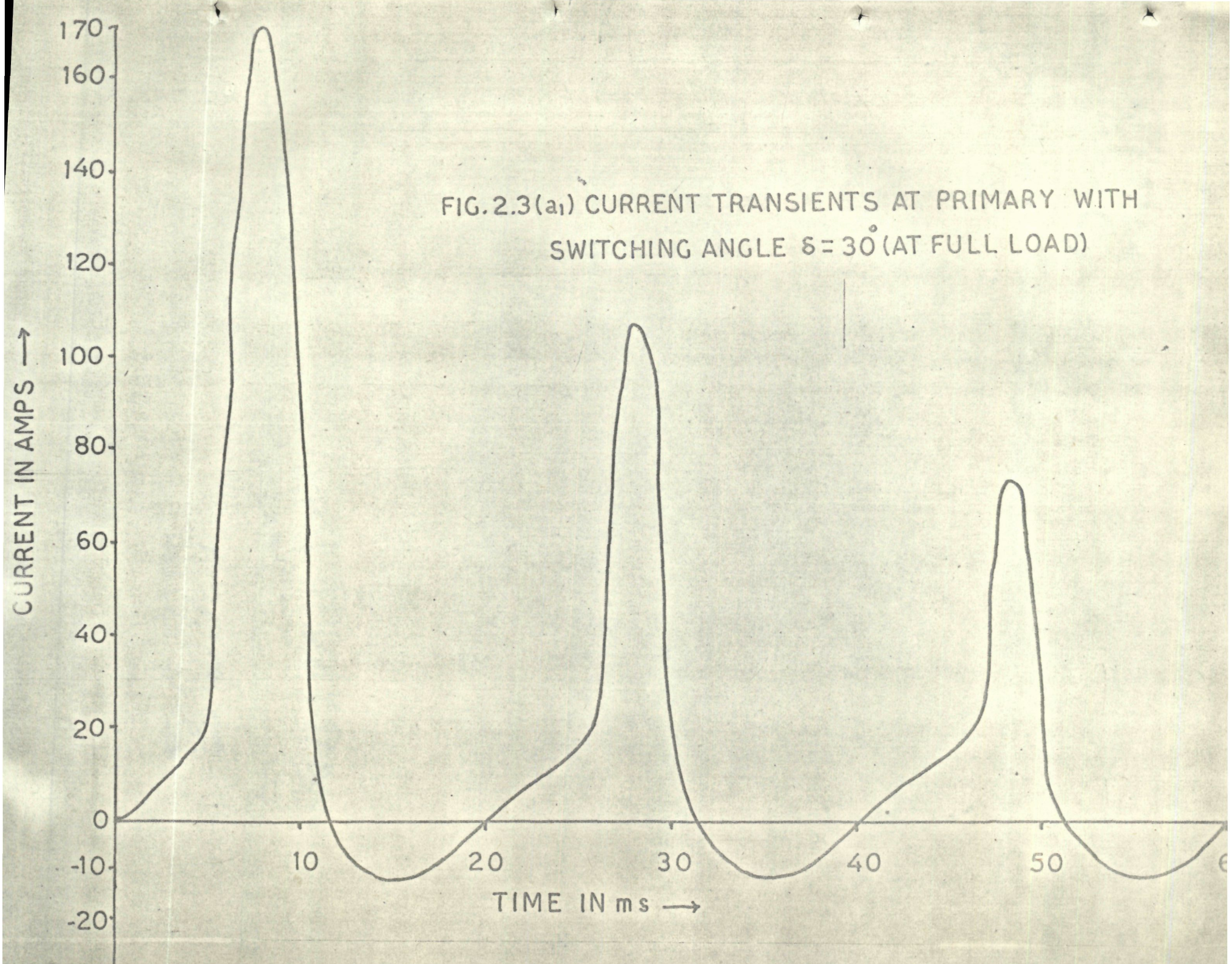
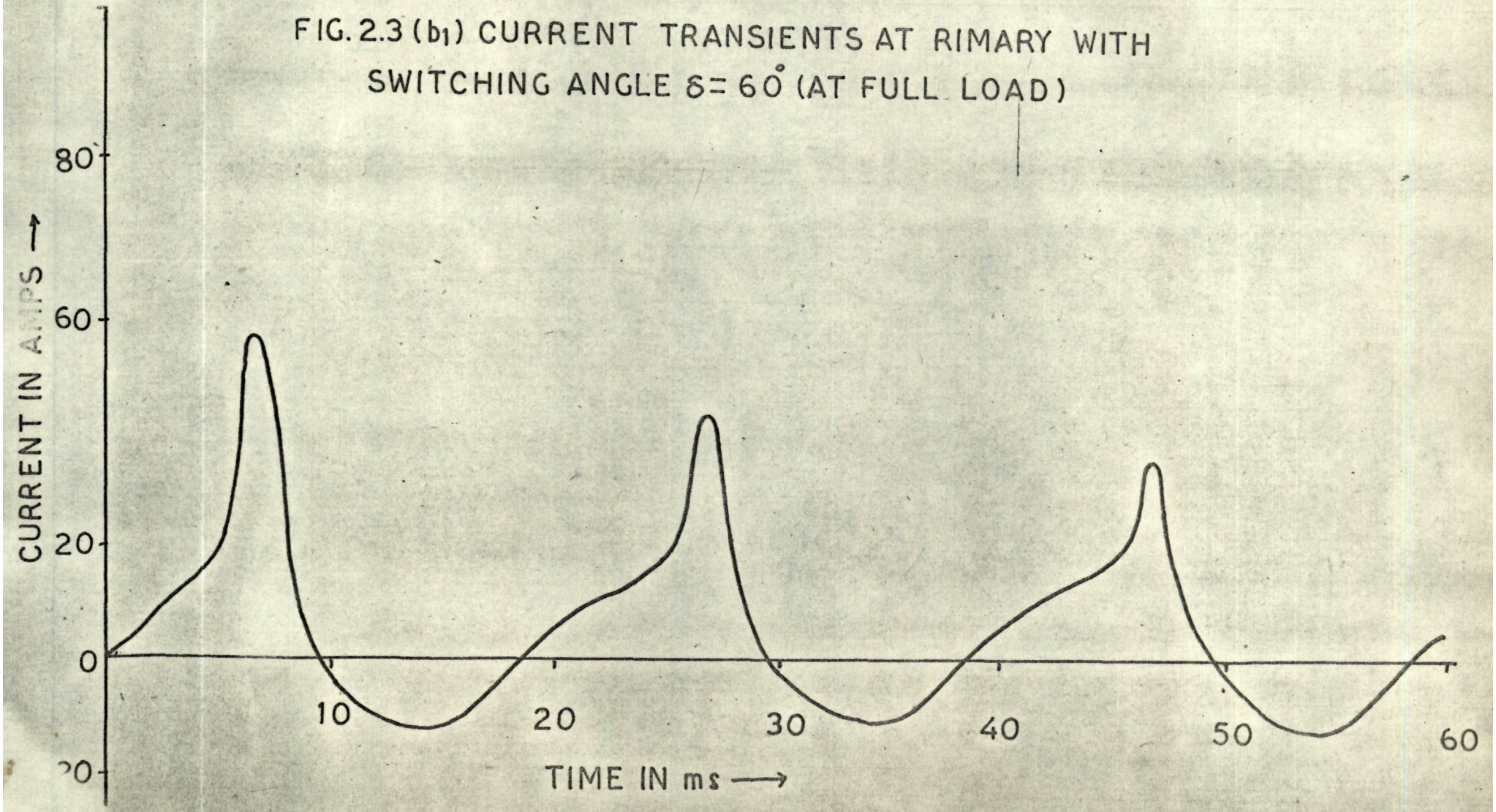


FIG. 2.3(a_1) CURRENT TRANSIENTS AT PRIMARY WITH SWITCHING ANGLE $\delta = 30^{\circ}$ (AT FULL LOAD)

FIG. 2.3 (b_1) CURRENT TRANSIENTS AT RIMARY WITH SWITCHING ANGLE $\delta = 60^{\circ}$ (AT FULL LOAD)



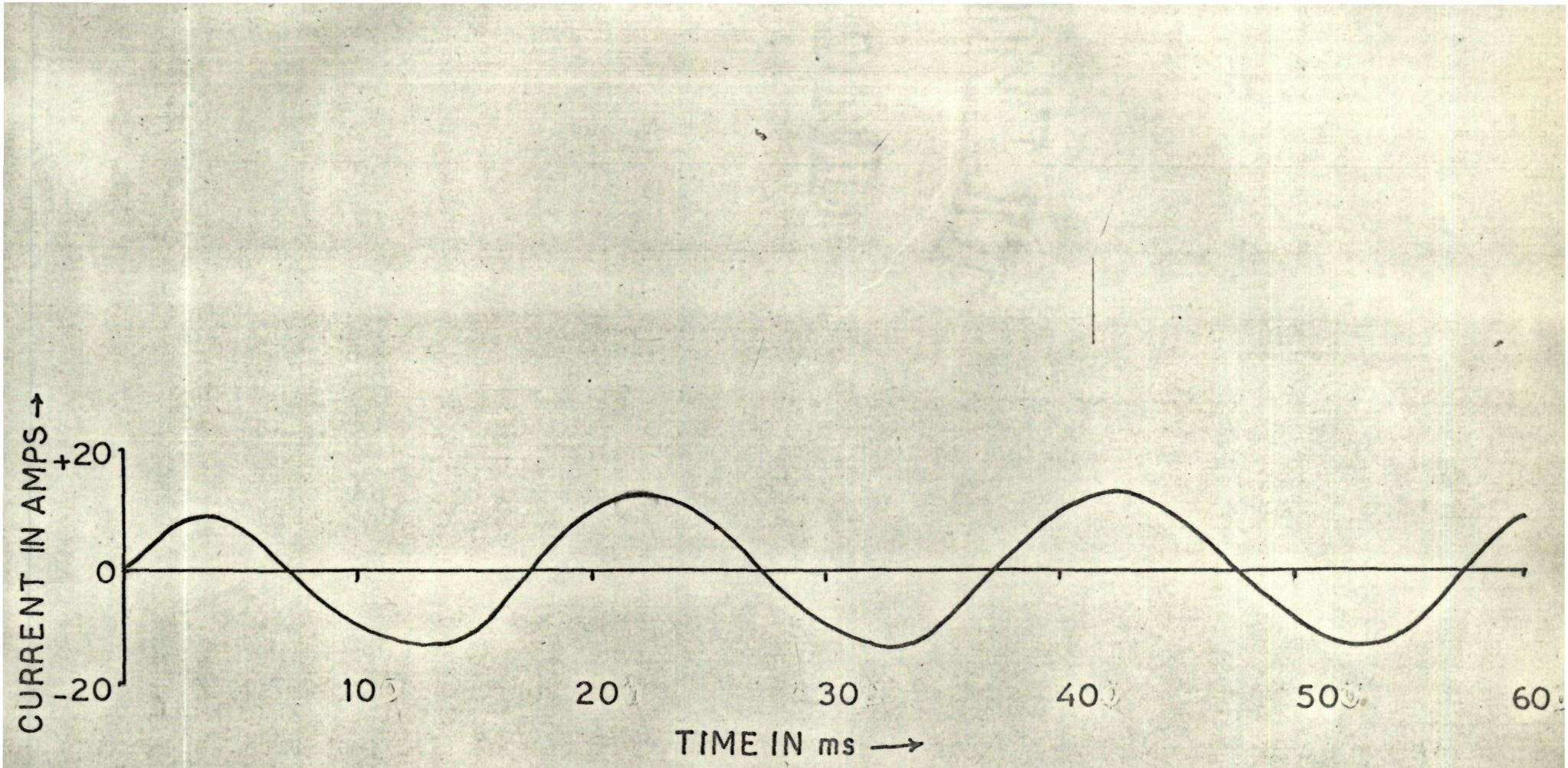


FIG 2.3(c_1) CURRENT TRANSIENTS AT PRIMARY WITH SWITCHING ANGLE $\delta = 90^{\circ}$ (AT FULL LOAD)

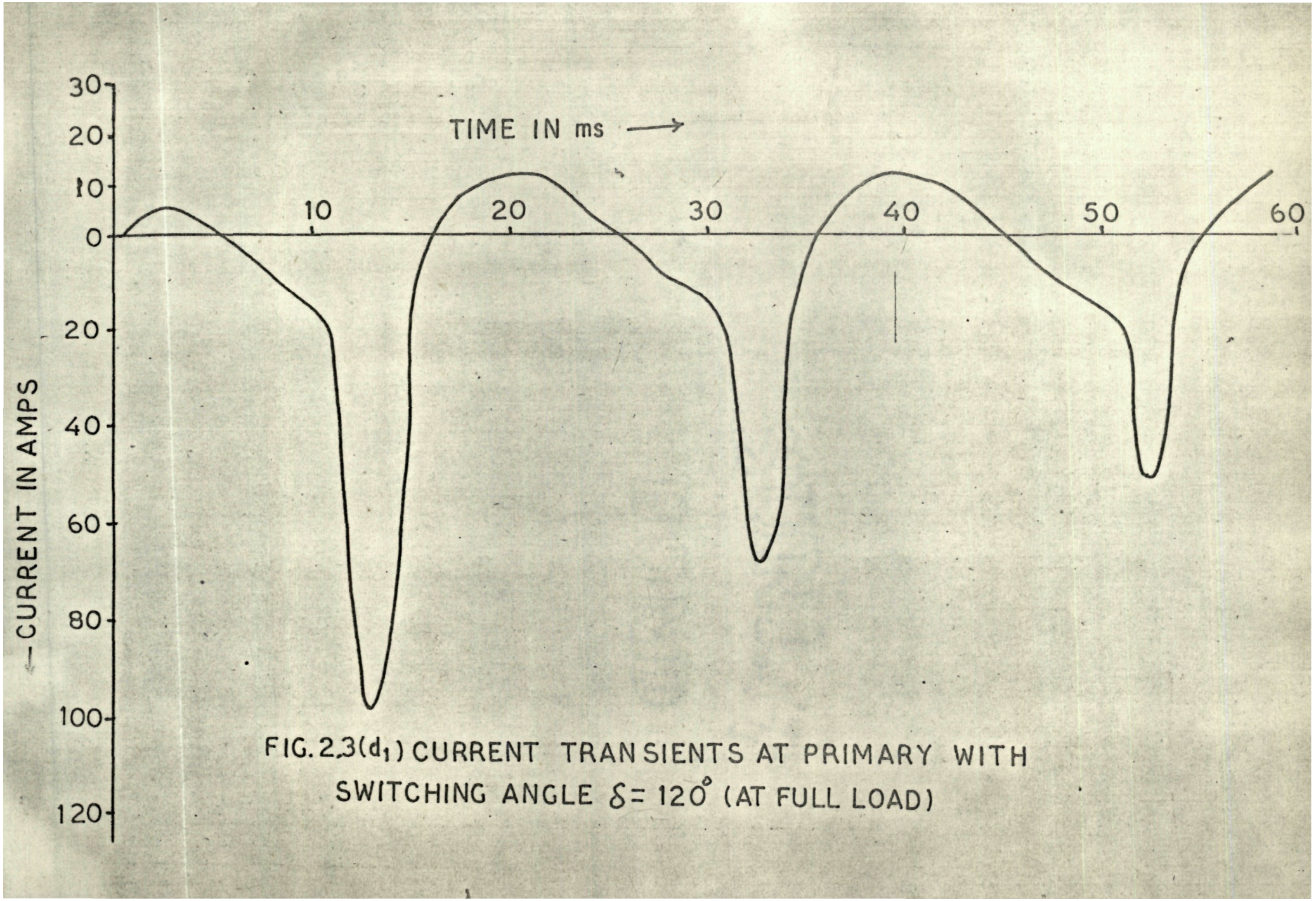


FIG. 2.3(d_1) CURRENT TRANSIENTS AT PRIMARY WITH SWITCHING ANGLE $\delta = 120^{\circ}$ (AT FULL LOAD)

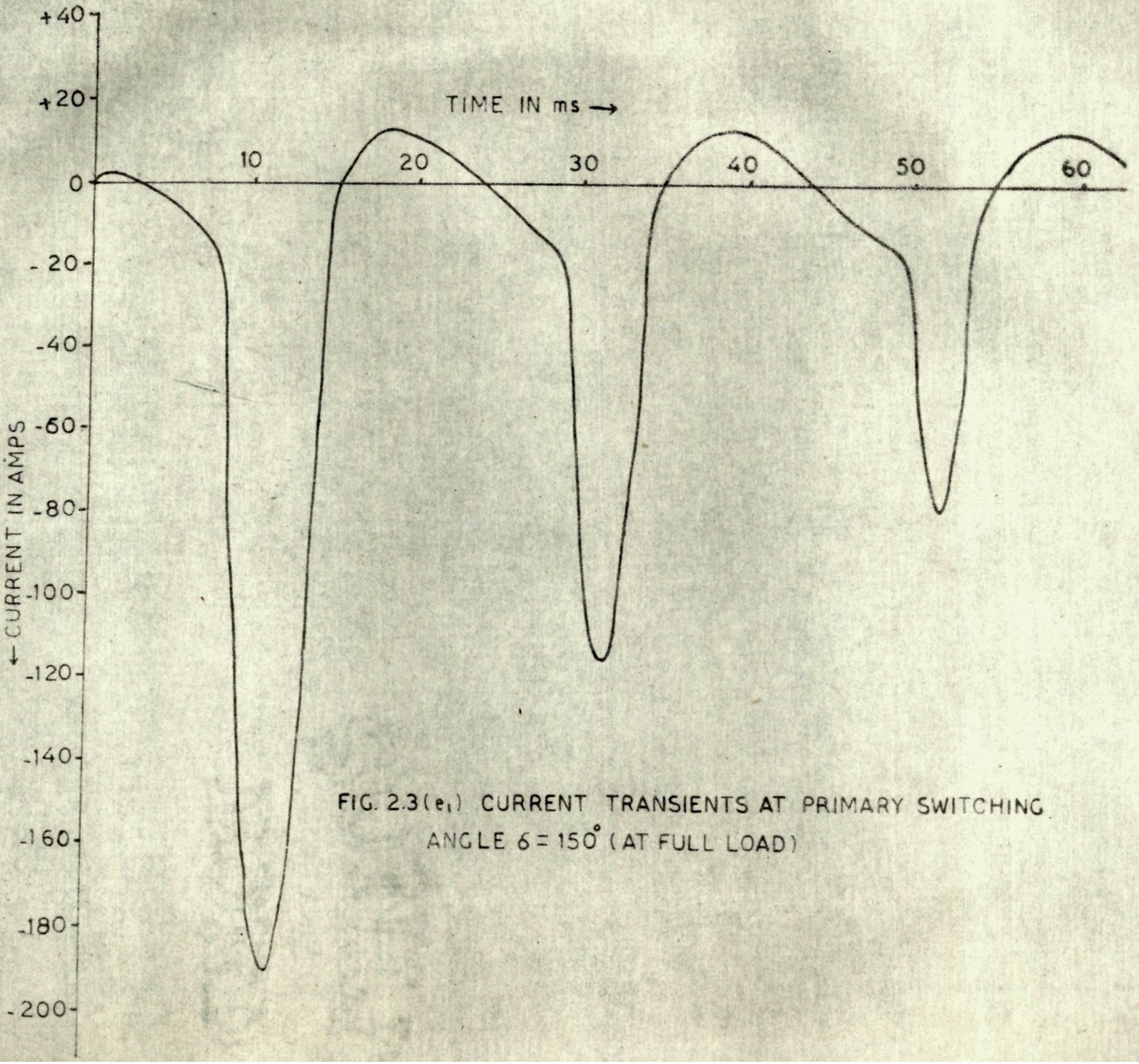


FIG. 2.3(e_1) CURRENT TRANSIENTS AT PRIMARY SWITCHING ANGLE $\delta = 150^\circ$ (AT FULL LOAD)

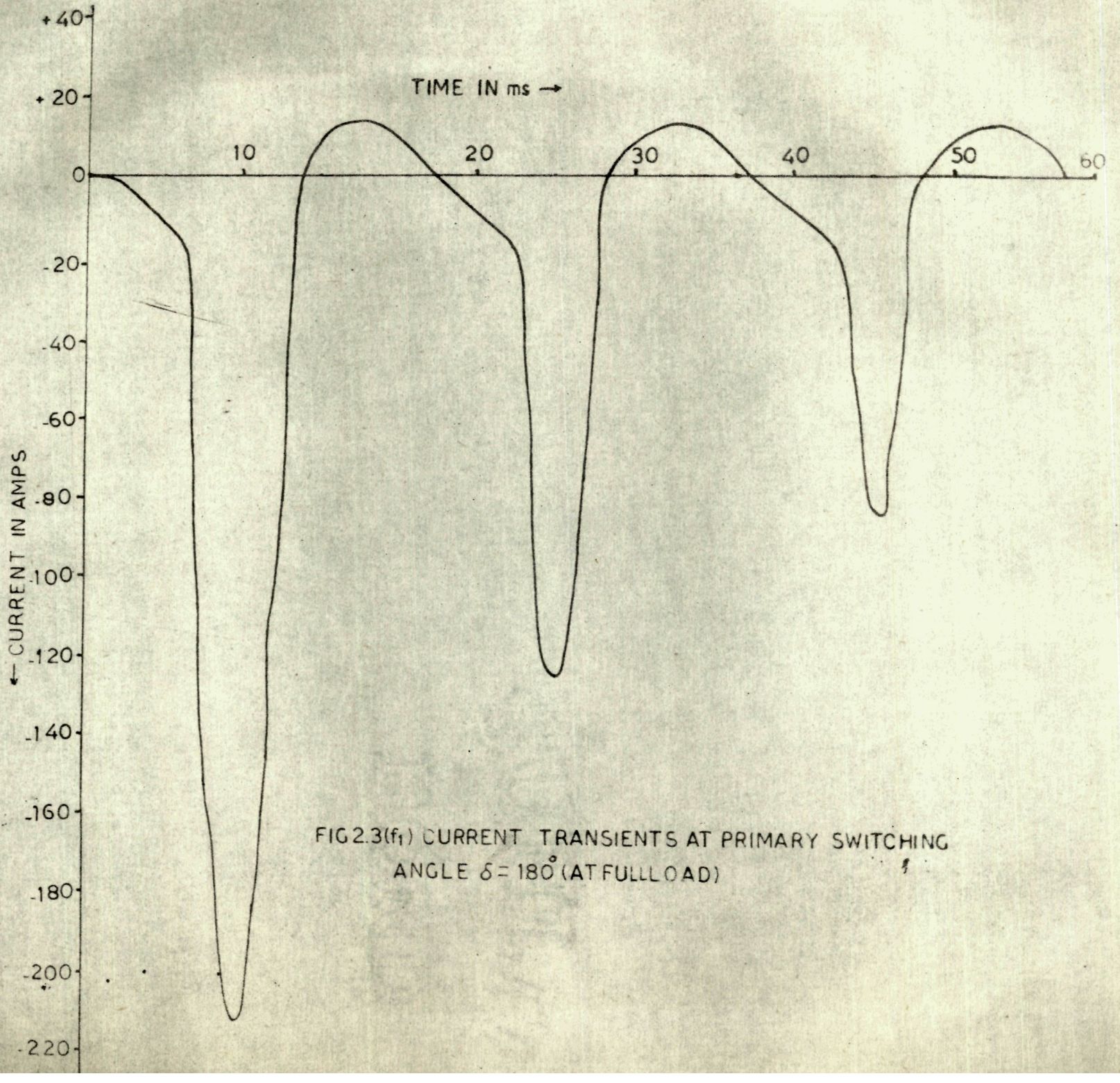


FIG 2.3(f_1) CURRENT TRANSIENTS AT PRIMARY SWITCHING ANGLE $\delta = 180^{\circ}$ (AT FULL LOAD)

It can be easily inferred from the above discussion and corresponding results (plotted in Fig.-2.3) that the inrush current in the transformer can be controlled by controlling the switching instant. The most appropriate instant of switching is at the peak value of the voltage.

In the following chapter a versatile electronic circuit is derived to switch-on the supply at any desirable instant in the range, 0^{o} to 180^{o} electrical. The circuit has been tested separately and then used to control the switching instant of a transformer and test results are obtained.

CHAPTER - 3

THE OUT-LINE OF THE PROPOSED SWITCHING SCHEME

THE OUT-LINE OF THE PROPOSED SWITCHING SCHEME

In this chapter an out-line of a scheme is proposed for obtaining a switching circuit with controlled switching instant. The basic principle is explained here. The detailed piecewise design of the complete circuit is given in the following chapter.

The most critical requirement in the proposed scheme is the generation of a control pulse at a predetermined instant during first half cycle of a sinusoidal voltage wave. This pulse can be used to trigger a switching device which closes the main power switch and keeps it closed in all subsequent cycles. As such the problem reduces to the generation of a control pulse after a desired period of time from the positive zero crossing instant of the voltage wave as shown in Fig.-3.1.

The time period between positive zero-crossing instant and the instant of appearance of the pulse can be controlled in either (i) by generating a pulse right at the positive zero crossing instant and then delaying of it for

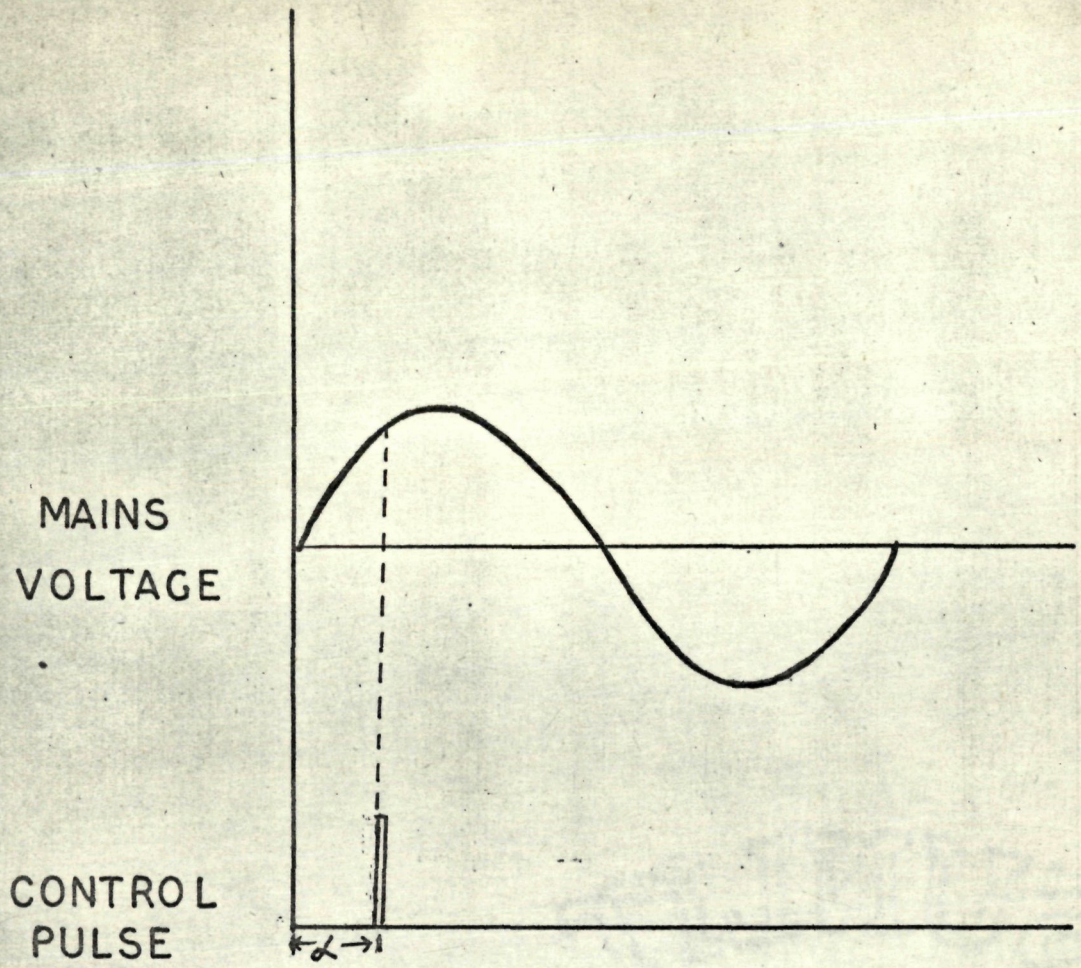


FIG. 3.1 PHASEANGLE OF CONTROL PULSE W.R.T. MAINS VOLTAGE

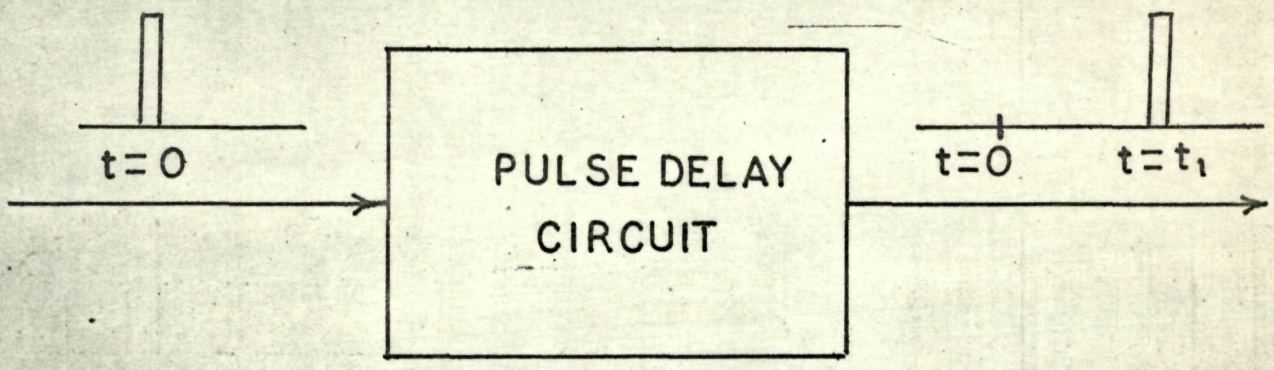


FIG. 3.2 PULSE DELAY CIRCUIT

a known period of time using monoshot or any other pulse delay circuit as shown in Fig.-3.2, or (ii) by generating a pulse after counting a known number of standard high frequency pulses from the zero crossing instant. The accuracy of the later scheme depends on the frequency and stability of high frequency pulse generator. For example each pulse of 18 KHz frequency signal corresponds to one degree of 50 Hz voltage wave. The first scheme suffers from the draw-back that the presence of monoshot in the circuit may lead to undesirable operation due to noise and stray pulses. Also a precise setting of delay period is difficult to obtain. Therefore the second method is chosen for realization in the present scheme.

An schematic diagram of the scheme is shown in Fig.-3.3. The first block is a Zero-Crossing-Detector (Z.C.D.) which produces logic '1' level corresponding to positive half cycle and logic '0' level corresponding to negative half cycle of the supply voltage wave. The square wave is used to reset a binary counter after each positive half cycle. The counter counts high frequency clock pulses

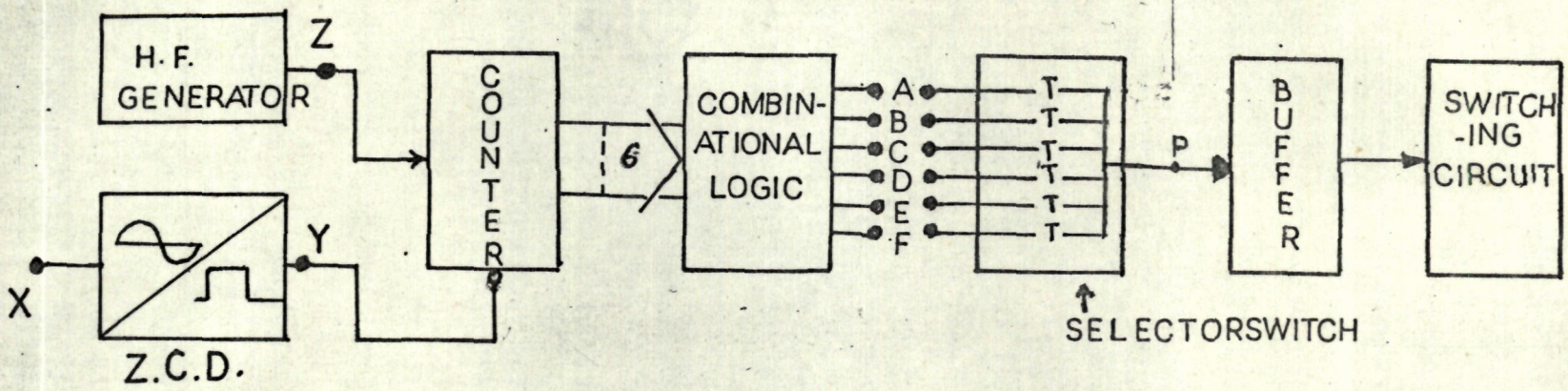


FIG_3.3 BLOCK DIAGRAM OF THE SWITCHING SCHEME

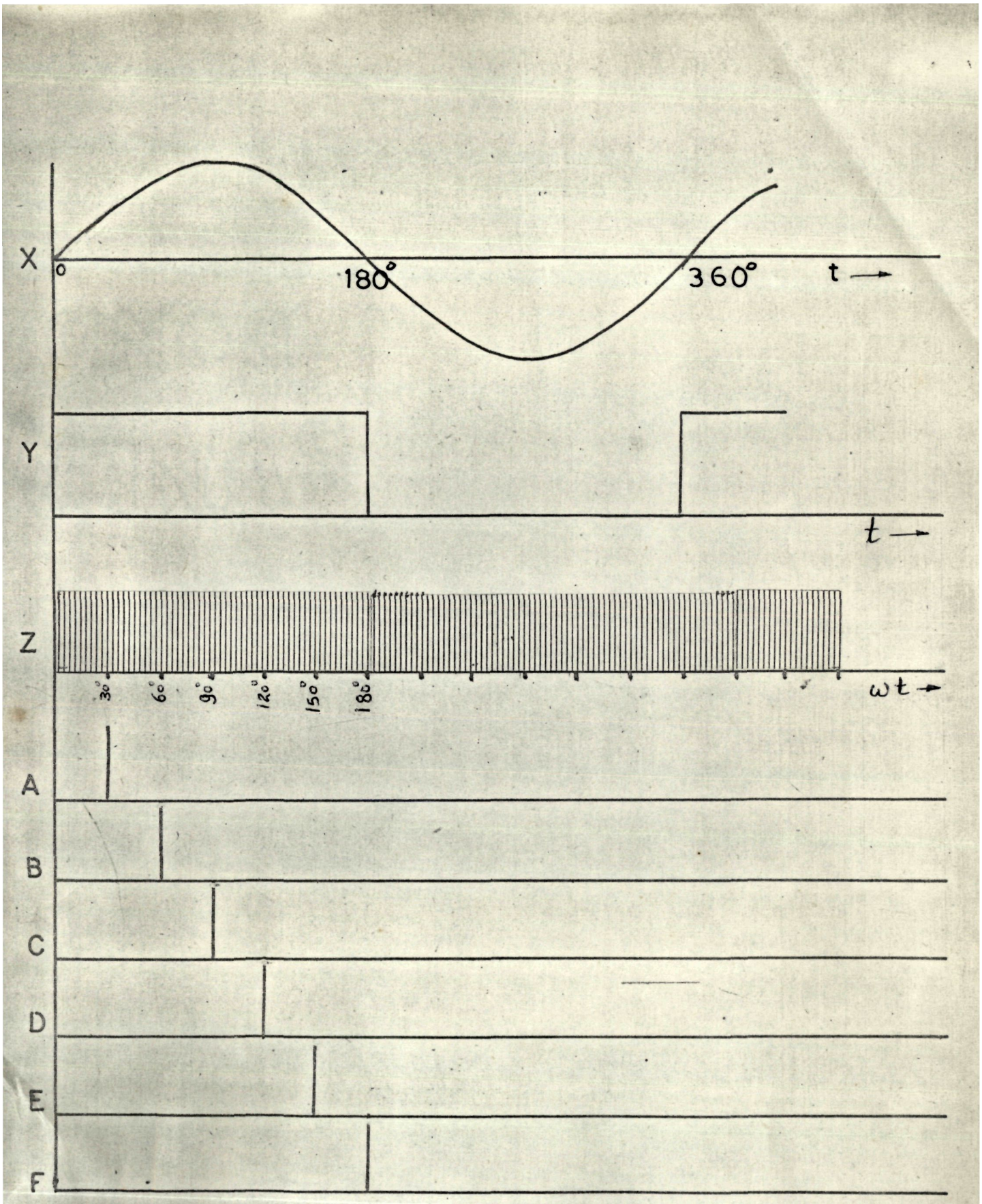


FIG. 3.4 TIMING DIAGRAMS OF VARIOUS TRIGGER SIGNALS

during each positive half cycle and then gets resetted at the trailing edge of the square wave from Z.C.D. The parallel outputs of the counter are connected to a combinational logic block which produces pulses at A, B, C, D, E and F after counting 10, 20, 30, 40, 50 and 60 pulses respectively. Now depending upon the desired switching instant any one of these outputs (i.e. A to F) is selected, buffered and used as trigger signal for the switching device. In the present work the designed frequency of high frequency generator is 6 KHz. Therefore each clock period corresponds to 3 degrees of 50 cycles voltage wave. If it is desired that the switch be closed at the instant corresponding to 30 degrees of the supply voltage cycle, then the signal A must be selected for triggering the switching device. Similarly for obtaining the switching instants corresponding to 60, 90, 120, 150 and 180 degrees the signals B, C, D, E and F respectively must be chosen for triggering the main power switch. The wave forms at important points of the block diagram are shown in Fig.-3.4 and the detailed design of each block is given in the following chapter.

CHAPTER - 4

DESIGN OF VARIOUS BUILDING BLOCKS

DESIGN OF VARIOUS BUILDINGS BLOCKS

In this chapter detailed design of various functional blocks mentioned in the previous chapter is given. It may be recalled that the required blocks for the proposed scheme are :

Zero Crossing Detector,

High Frequency Pulse Generator,

Trigger Circuit,

Binary Counter,

Combinational Logic,

Selector Switch,

Buffer Stage,

Switching Circuit, and

Power Supplies.

4.1. Zero Crossing Detector

An operational Amplifier μA741 in open loop mode is used as Zero Crossing Detector (Z.C.D.). Since the open loop gain of operational amplifier (Op.-Amp.) is very high ($\simeq 10^6$) even a very small

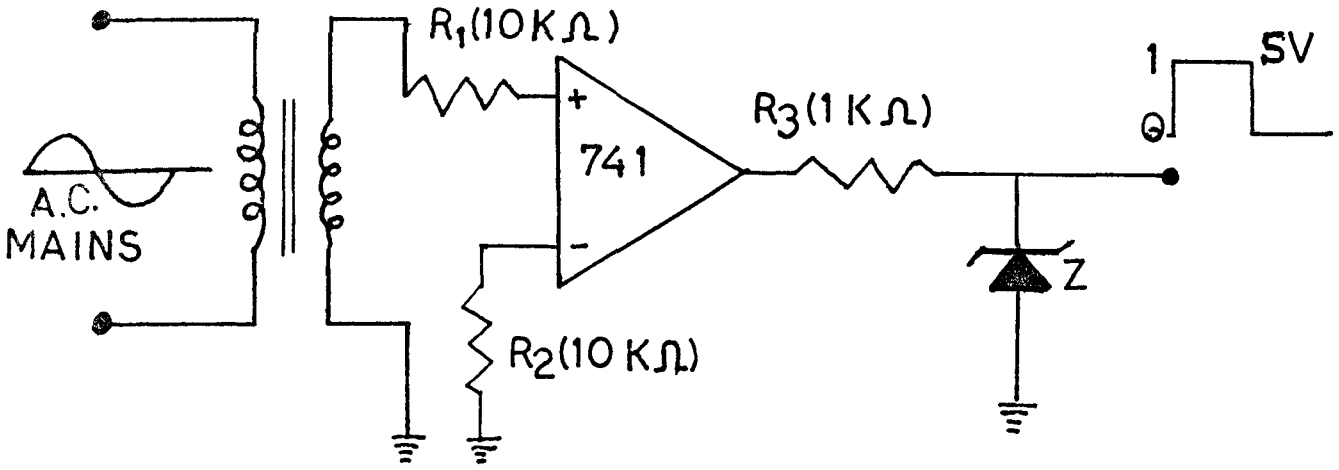


FIG-4.1 ZERO CROSSING DETECTOR

differential voltage at the input will cause its output to saturate to either positve or negative maximum voltages[8]. The output voltage is limitted to +5 Volt and O Volt by connecting a zener diode after resistance R . Thus a sinusoidal wave is converted into a ractangular wave, with high level (Logic '1') during positive half cycle and low level (Logic 'O') during negative half cycle of the mains voltage. Designed values of circuit elements are indicated in Fig.-4.1.

4.2. High Frequency Pulse Generator

A 6 KHz H.F. pulse generator is considered to give sufficiently accurate switching instant for switching-on a transformer. Timer NE/SE 555 is used in astable mode to give these high frequency pulses. The frequency of operation depends very little on supply voltage magnitude (according to manufacturer's data sheet; timing drift is approximately O.Ol percent per volt)[11]. Pin No. 4 and 8 are connected to V_{cc} and pin No. 1 to ground. Pin No. 2 and 6 are connected

together and to a capacitor C. Two series resistors R_a and R_b are used to charge the capacitor through V_{cc}. Pin No. 7 is connected to the junction point of these resistors. During charging period as the capacitor voltage reaches 2/3rd of V_{cc}, pin No. 7 is internally connected to ground, the potential at this pin immediately falls to zero, and the capacitor starts discharging through R_b. Now as soon as the potential of capacitor reaches 1/3rd of V_{cc}, pin No.7 is again internally disconnected from ground and can assume any positive voltage depending on external circuit. This cyclic charging and discharging of the capacitor through $(R_a + R_b)$ and R_b respectively, continues so long as a voltage source V_{cc} is present.

The frequency of oscillation at the output is

$$f = \frac{1.44}{(R_a + 2R_b)C} \text{ KHz}$$

where R_a and R_b are in Kilo-Ohm and C in Micro-Farad. The designed values of circuit elements are indicated in Fig.-4.2.

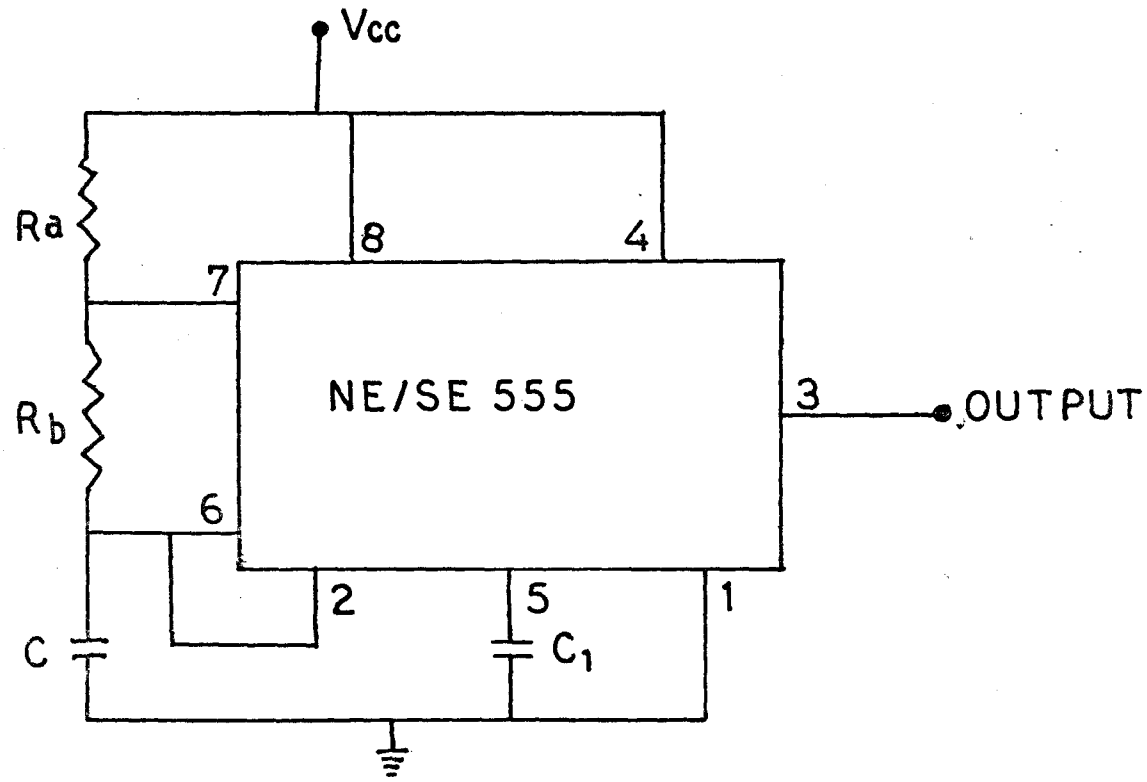


FIG_4.2 HIGH FREQUENCY PULSE GENERATOR

4.3. Trigger Circuit

As the instant of switching-on in the first power cycle is of interest, the counter should not start counting from any randum instant as soon as supply is switched-on. It must be ensured that the counter starts counting only at the front edge of the output of Z.C.D. i.e. from the instant at which the mains voltage changes its polarity from negative to positive as shown in Fig.-4.3. A trigger circuit designed around NE/SE 555 timer is used for this purpose. The circuit used is given in Fig.-4.4.

Pin No.4 is normally connected to ground to keep the chip disabled and connected momentarily to V_{cc} when triggering is required. Output of Z.C.D. is connected to pin No.2 which triggers the timer output to high level at trailing edge. But as the desired triggering instant is front edge, Z.C.D. output and timer output are connected to an AND gate which gives a high output when Z.C.D. output again goes from low to high level (i.e. front edge).

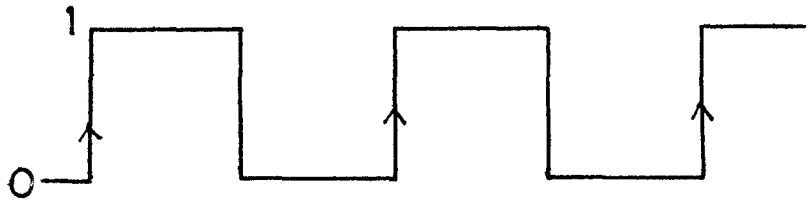


FIG_4.3 OUTPUT OF Z.C.D.

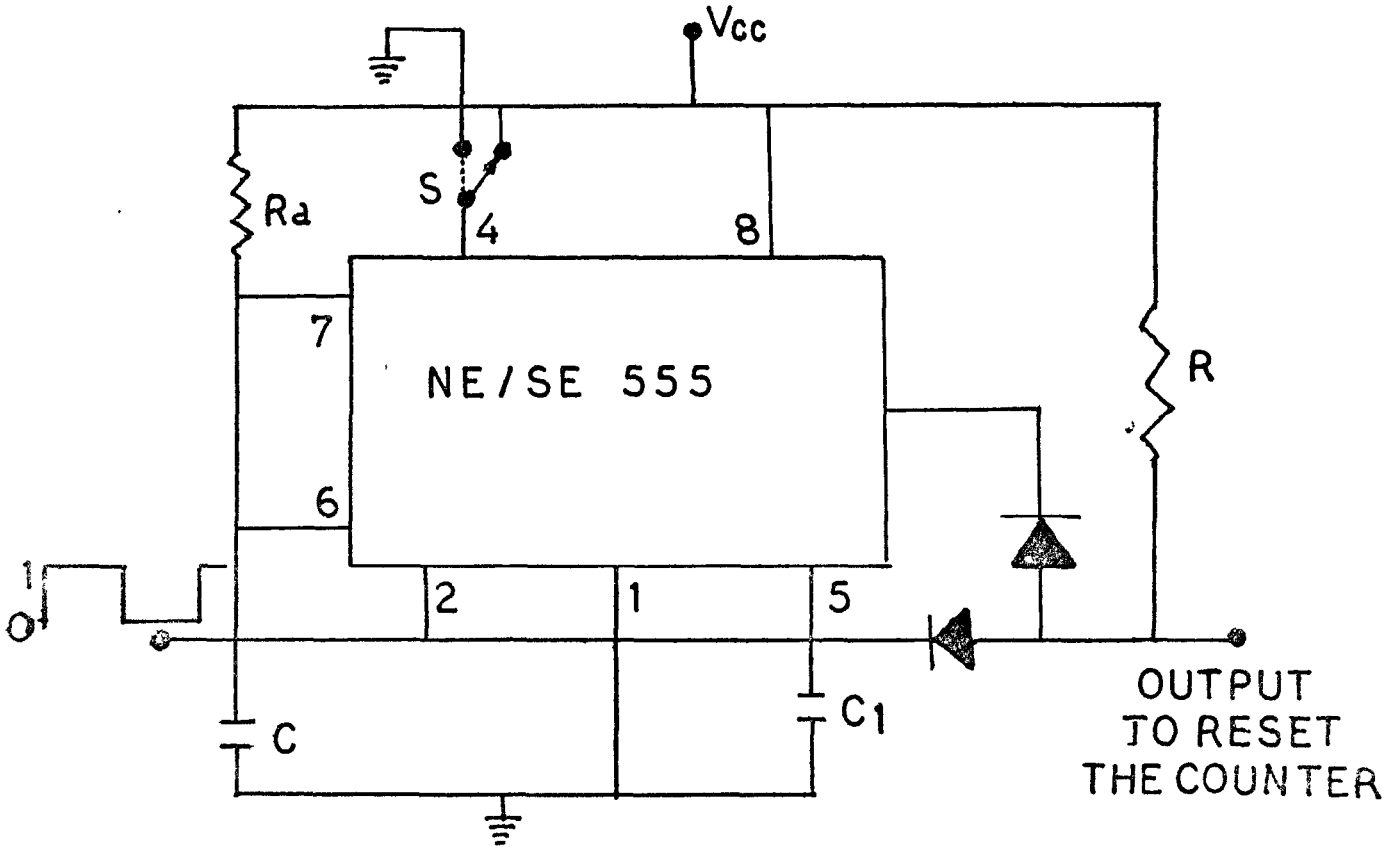


FIG_4.4 TRIGGER CIRCIUT

4.4. Binary Counter[9]

Two IC chips (Sp.No. DM 7493 AN) of binary counter each having 4 bits output are used to count the number of pulses from H.F. Generator. The maximum number of 6 KHz frequency pulses available in half positive cycle of supply voltage is 60, thus the counter has to count in the range from 0 to 60 pulses. Therefore out of the combined 8 bits output of the counter, only first 6 bits are sufficient to count in this range, remaining 2 bits are left unconnected the chips are arranged as shown in Fig.-4.5.

Q_{A_1}, Q_{B_1}, Q_{C_1}, Q_{D_1}, Q_{A_2}, Q_{B_2} are the 6 binary outputs of the counter. Q_{A_1} forms LSB where as Q_{B_2} forms MSB of the binary output. The counting sequence is shown in Table-1.

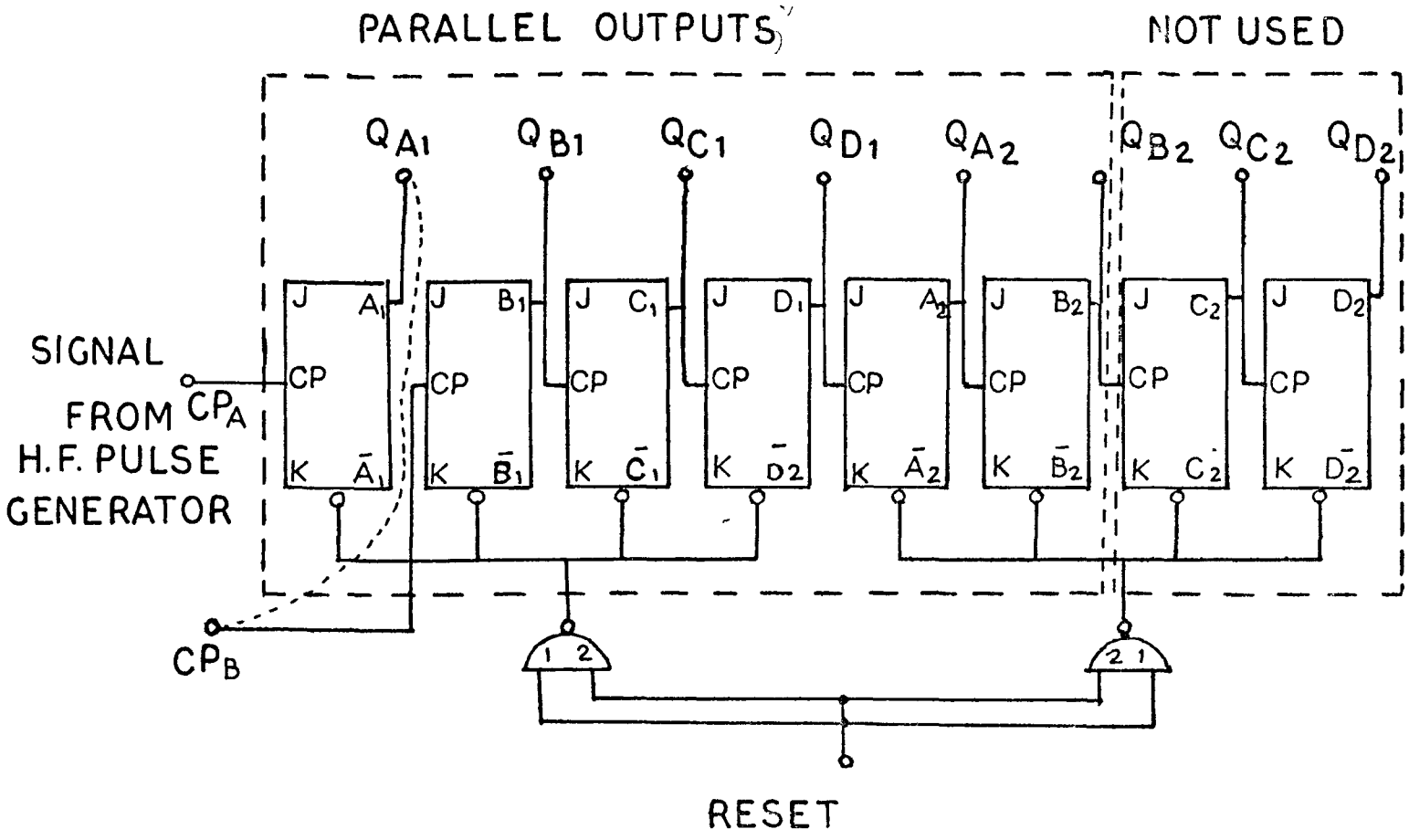


FIG. 4.5. 6-BIT BINARY COUNTER

TABLE - 1

Pulse Number	Q_{B_2}	Q_{A_2}	Q_{D_1}	Q_{C_1}	Q_{B_1}	Q_{A_1}
0	0	0	0	0	0	0
1	0	0	0	0	0	1
2	0	0	0	0	1	0
3	0	0	0	0	1	1
4	0	0	0	1	0	0
5	0	0	0	1	0	1
6	0	0	0	1	1	0
7	0	0	0	1	1	1
8	0	0	1	0	0	0
9	0	0	1	0	0	1
10	0	0	1	0	1	0
11	0	0	1	0	1	1
12	0	0	1	1	0	0
13	0	0	1	1	0	1
14	0	0	1	1	1	0
15	0	0	1	1	1	1
16	0	1	0	0	0	0
17	0	1	0	0	0	1
18	0	1	0	0	1	0
19	0	1	0	0	1	1
20	0	1	0	1	0	0

21	0	1	0	1	0	1
22	0	1	0	1	1	0
23	0	1	0	1	1	1
24	0	1	1	0	0	0
25	0	1	1	0	0	1
26	0	1	1	0	1	0
27	0	1	1	0	1	1
28	0	1	1	1	0	0
29	0	1	1	1	0	1
30	0	1	1	1	1	0
31	0	1	1	1	1	1
32	1	0	0	0	0	0
33	1	0	0	0	0	1
34	1	0	0	0	1	0
35	1	0	0	0	1	1
36	1	0	0	1	0	0
37	1	0	0	1	0	1
38	1	0	0	1	1	0
39	1	0	0	1	1	1
40	1	0	1	0	0	0
41	1	0	1	0	0	1
42	1	0	1	0	1	0
43	1	0	1	0	1	1
44	1	0	1	1	0	0
45	1	0	1	1	0	1

46	1	0	1	1	1	0
47	1	0	1	1	1	1
48	1	1	0	0	0	0
49	1	1	0	0	0	1
50	1	1	0	0	1	0
51	1	1	0	0	1	1
52	1	1	0	1	0	0
53	1	1	0	1	0	1
54	1	1	0	1	1	0
55	1	1	0	1	1	1
56	1	1	1	0	0	0
57	1	1	1	0	0	1
58	1	1	1	0	1	0
59	1	1	1	0	1	1
60	1	1	1	1	0	0

Pin diagram and other relevant information of the counter chip are given in Appendix (B).

4.5. Combinational Logic

In order to produce control pulses after 10, 20, 30, 40, 50 and 60 counts, combinational logic circuit comparising suitable logic gates should be connected

at the output of the counter. Out of the six binary outputs of the counter, few are selected to be used as inputs to various AND gates in order to get control pulses after desired counts. The outputs used are as shown in Table-2, and their connections are shown in Fig.-4.6.

TABLE - 2

Inputs to Combinational Logic	Designed pulse Counts
Q_{D_1} and Q_{B_1}	10
Q_{A_2} and Q_{C_1}	20
Q_{A_2}, Q_{D_1}, Q_{C_1} and Q_{B_1}	30
Q_{B_2} and Q_{D_1}	40
Q_{B_2}, Q_{A_2} and Q_{B_1}	50
Q_{B_2}, Q_{A_2}, Q_{D_1} and Q_{C_1}	60

Three IC chips of Quard-2 input AND gate (DM 7408 N) and one chip of Triple-3 input AND gate (DM 7411 N) are used for realization of the combina-

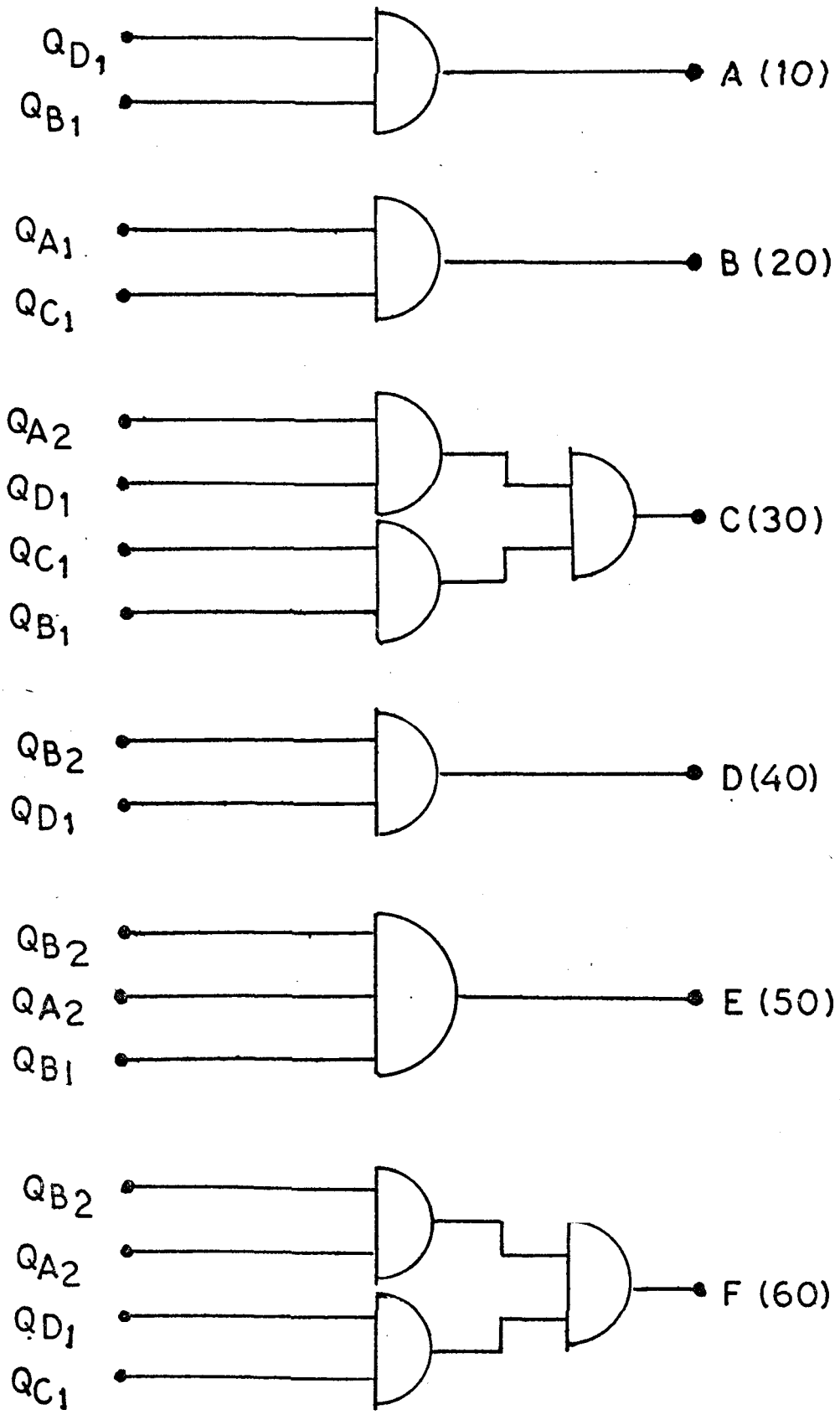


FIG_4.6 COMBINATIONAL LOGIC

tional logic circuit. The IC pin diagrams are shown in Appendix (C).

4.6. Selector Logic

It is to be noted that out of these six control pulses available at the outputs of combinational logic, only one pulse has to be used at a time for triggering the switching device. To select particular output line a selector logic consisting of AND gates is used. Combinational logic outputs A to F form one of the inputs to two input AND gates. The 2nd input of each gate is connected to toggle switches S_1 to S_6 respectively.

The outputs of all AND gates are connected together after a diode in each output line. The switch corresponding to selected output is kept at position V_{cc} while the remaining switches are kept at ground position. The arrangement of these gates is shown in Fig.-4.7.

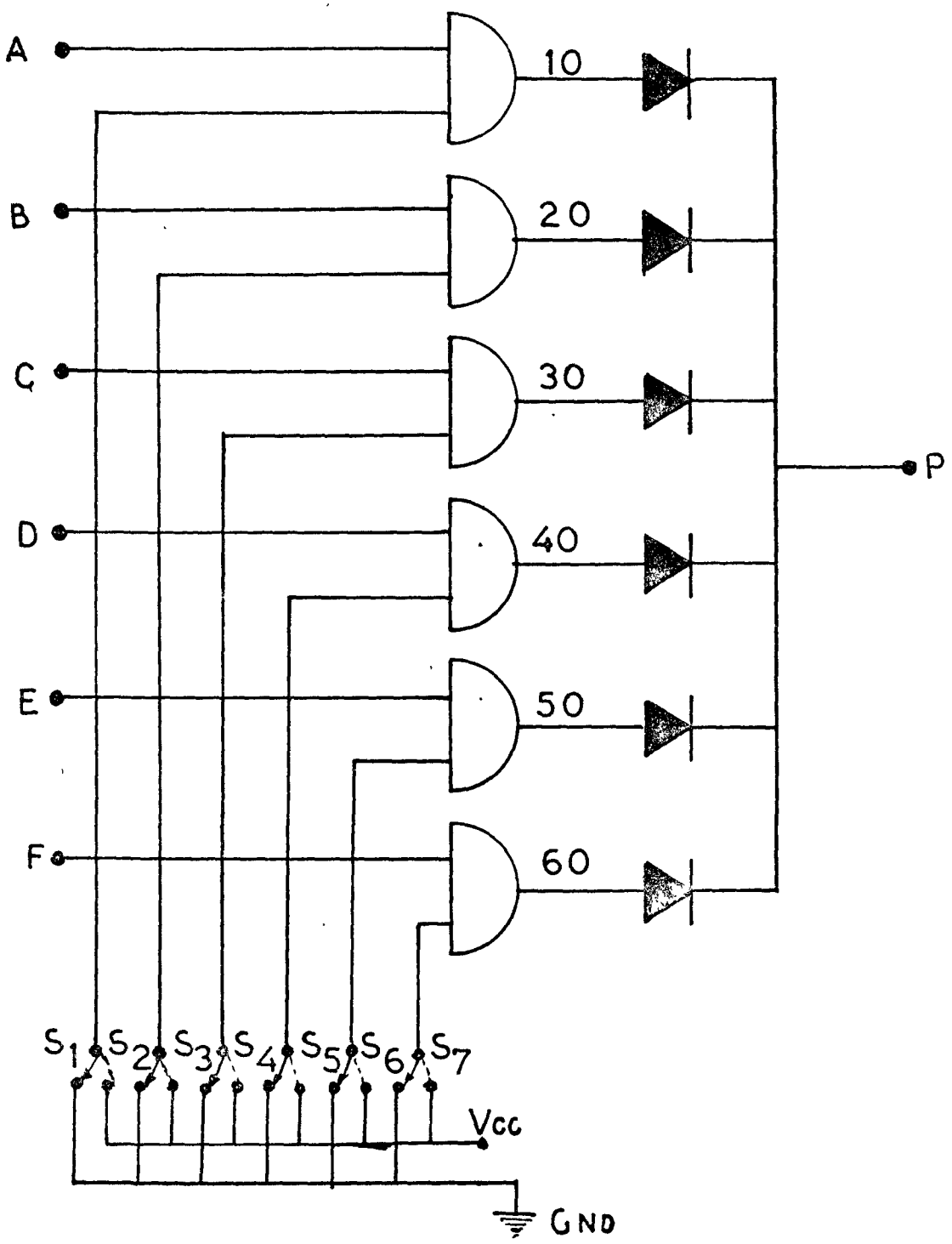


FIG. 4.7 SELECTOR LOGIC

4.7. Buffer Stage[10]

The TTL output level available at point P is usually not sufficient to trigger the switching circuit reliably. The triggering gate current required for a medium range SCR may vary from few mA to few 10s of mA. It is advisable to connect a buffer stage between IC's output and power circuit. An n-p-n transistor is used as emitter follower to form a buffer stage. The circuit is shown in Fig.-4.8.

A 1:1 pulse transformer is used to isolate the control circuit from power circuit.

4.8. Switching Circuit

The control pulse after proper buffering and isolation is used to trigger the power switch. This pulse is used just as a starting signal for commencement of conduction and once the switch starts conducting, it should stay-on parmanently.

The circuit being AC, requires a bidirectional controlled switch for conduction in both cycles. The

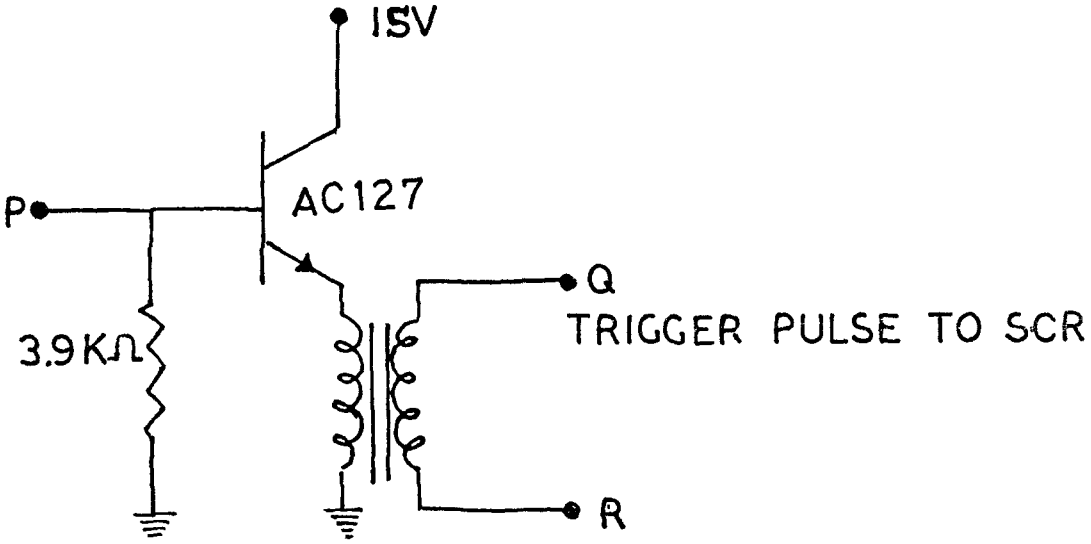


FIG 4.8 BUFFER CIRCUIT

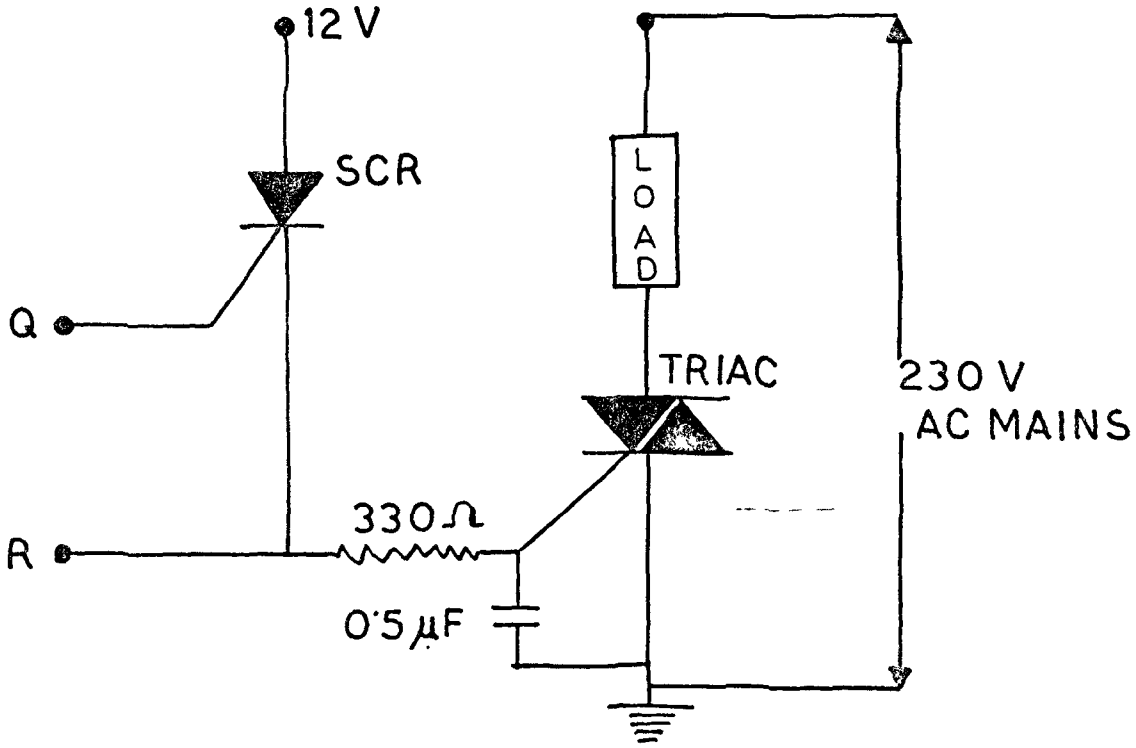


FIG. 4.9 MAIN SWITCHING BLOCK

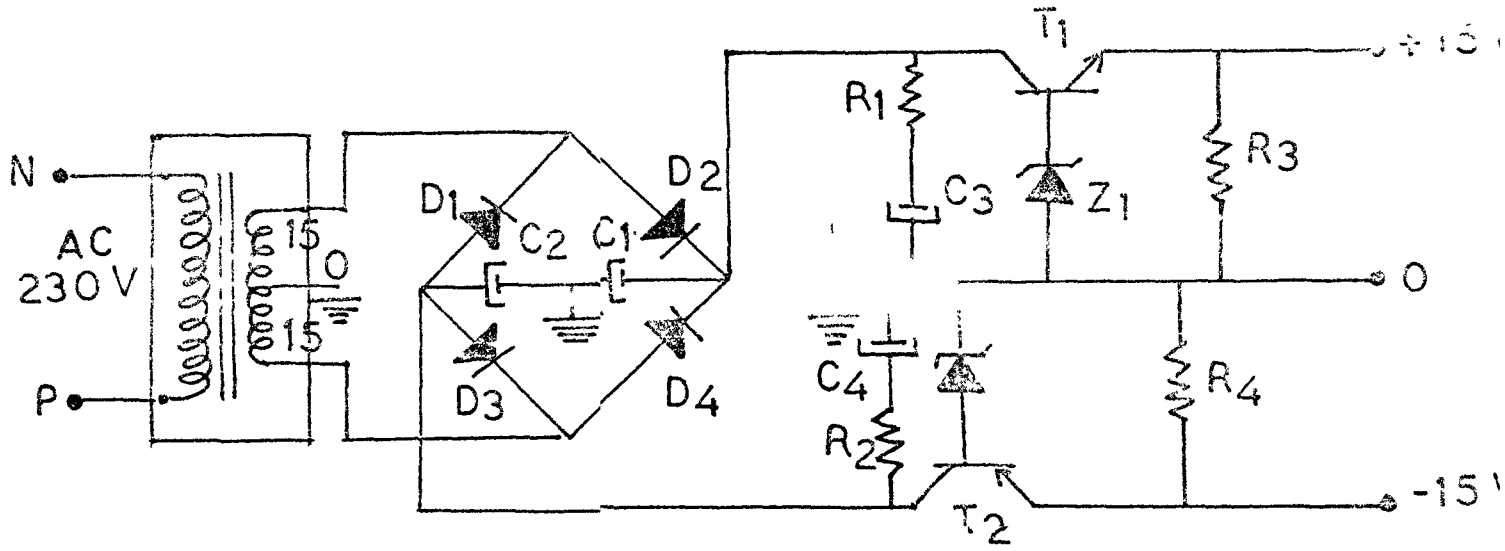
trigger signal is applied in two stages viz., first of all the control signal turns-on an SCR which in-turn supply permanent gate-supply through the SCR keeps the triac-on in all subsequent cycles[8]. The circuit diagram is shown in Fig.-4.9.

4.9. Power Supplies

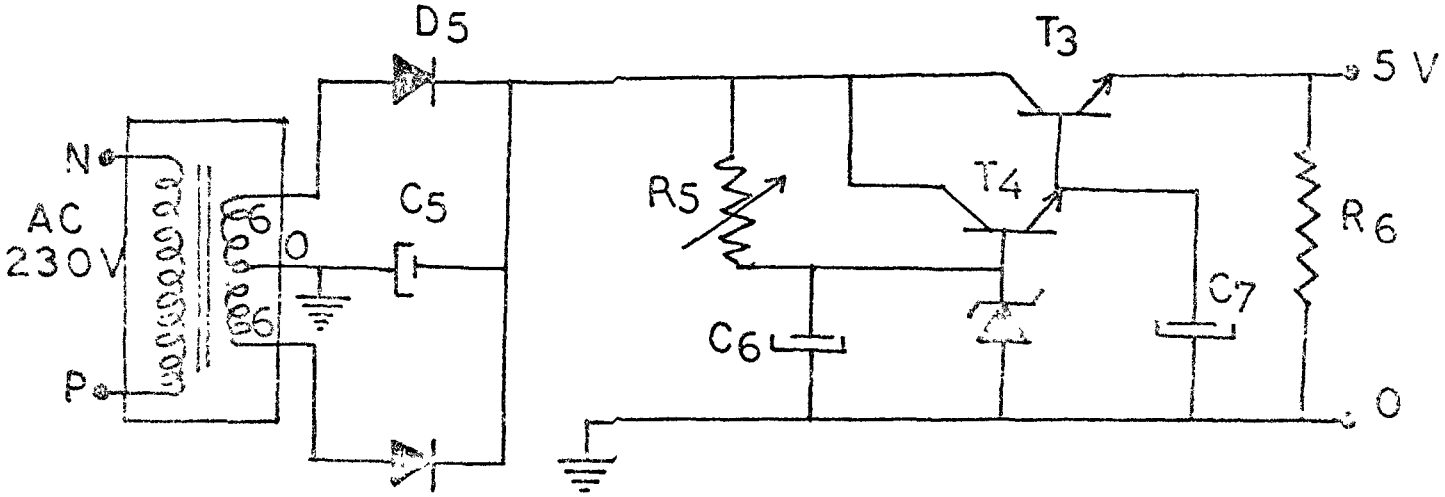
All three power supplies used in the entire circuit, are also designed, fabricated in the lab. and incorporated with the scheme.

No external power supply is required and the circuit works with 230 volts AC mains. +5 V and ±15 V are stabilized d.c. voltage sources, whereas +12 V supply is without stabilization means. The circuit diagrams are shown in Fig.-4.10, and design details are given in Appendix (D).

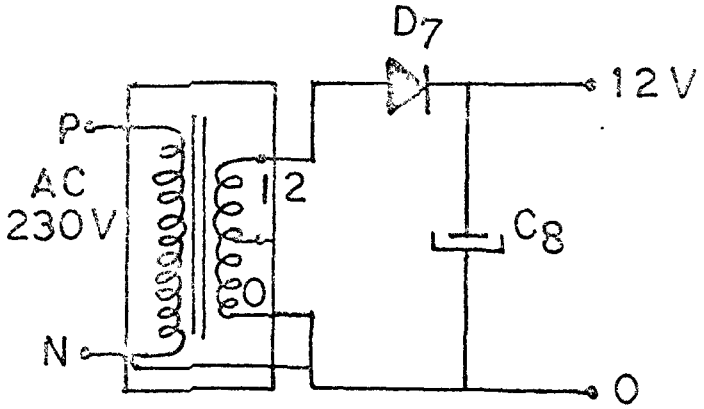
A complete detailed circuit diagram of controlled instant switching scheme is shown in Fig.-4.11. The layout diagram of Card (A) is also given in Appendix(D).



(A) ± 15 VOLT SUPPLY



(B)+ 5 VOLT SUPPLY



(C) 12 VOLT SUPPLY

FIG.4.10 POWER SUPPLIES

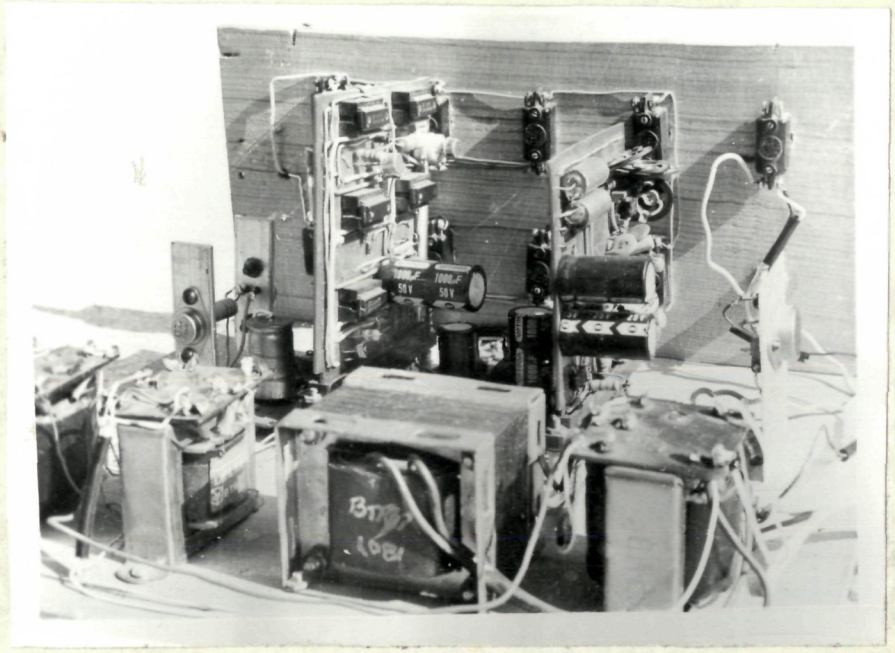


Fig.4.12 SIDE VIEW OF FABRICATED CIRCUIT.

CHAPTER - 5

TESTING AND EXPERIMENTAL RESULTS

TESTING AND EXPERIMENTAL RESULTS

5.1. Manual Testing of the Circuit

The operation of the scheme was first demonstrated after having some modifications in the initial blocks, so that to have a feel of working of the circuit. This part of testing is referred to as manual testing. Actual testing (Auto-testing) is followed by this preliminary testing.

In manual testing a low frequency generator is connected in place of high frequency generator. The frequency of this pulse generator is kept very low so as to enable visual counting of pulses with the help of an LED at the output. For this purpose the triggering arrangement is also replaced by a reset switch. The design details of the low frequency pulse generator are given in the Appendix (E).

During manual testing it was seen that after application of reset pulse, the power switch turned-on

after the completion of set number of pulses. The circuit was found to work satisfactorly at all settings.

5.2. Actual Testing of the Circuit

Actual testing (Auto-mode) was performed by studying the switching instant of supply to a resistive load. Photographic records of the current wave for different settings of the selectors were taken. First one cycles of the results were enlarged and switching instants measured and were found to be in close confirmity of the designed values.

5.3. Switching Transients of the Transformer

Once the working of the circuit was verified by manual as well as auto-testing with resistive load, it was then used to switch on the open circuited transformer at different desired instants. The photegraphic results are included here.

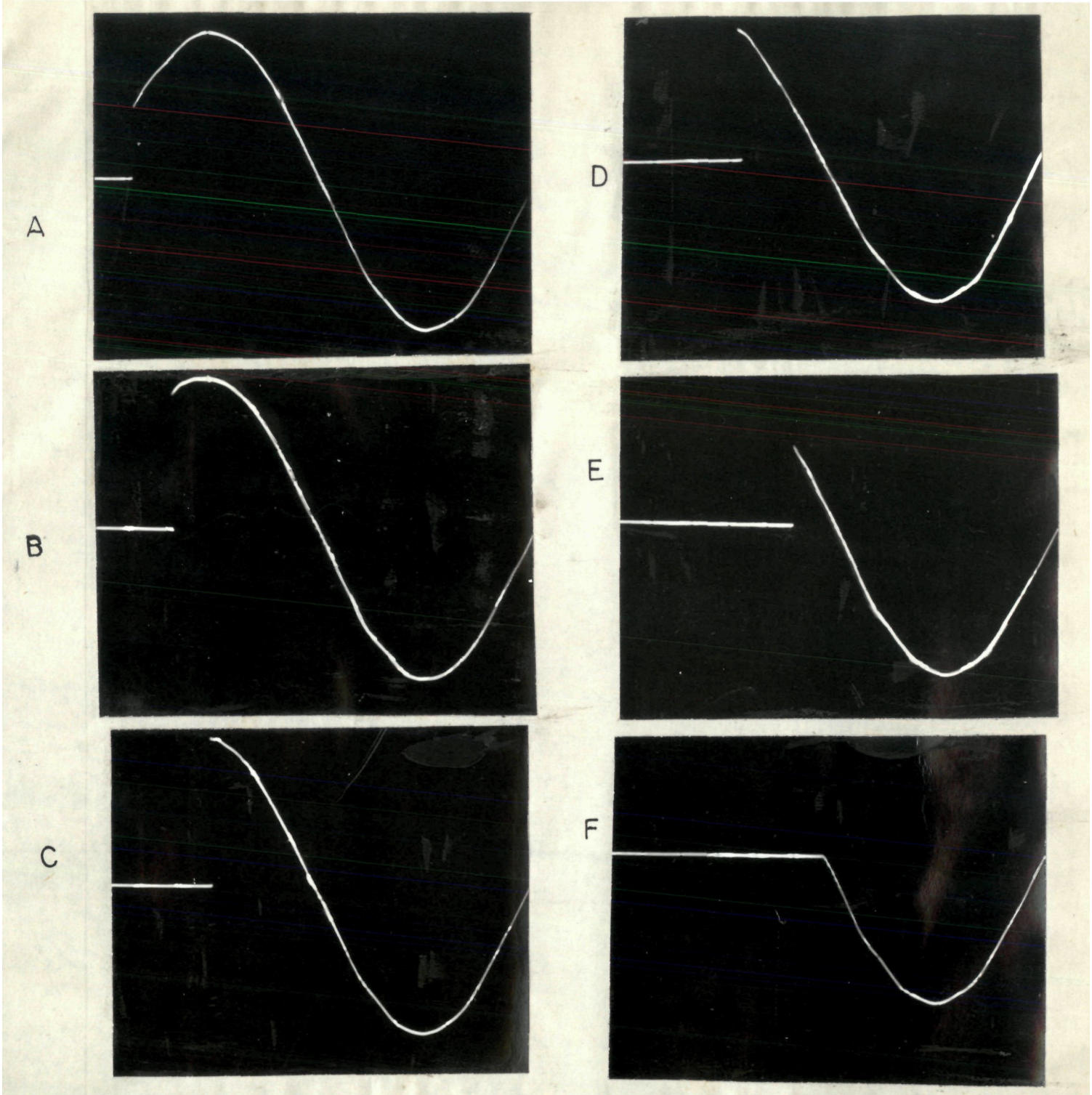


Fig.5.2 Photograph of First Cycle of Applied Voltage with Different Switching Instants.

[A] Switching Angle $\partial = 30^{\circ}$

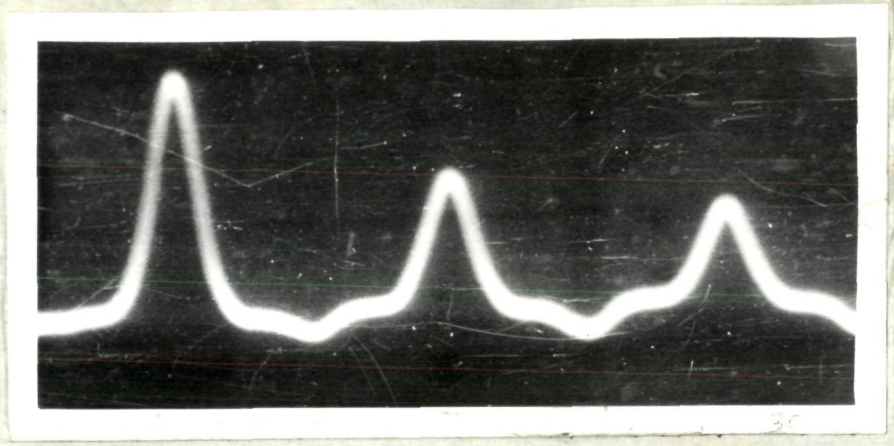
[B] Switching Angle $\partial = 60^{\circ}$

[C] Switching Angle $\partial = 90^{\circ}$

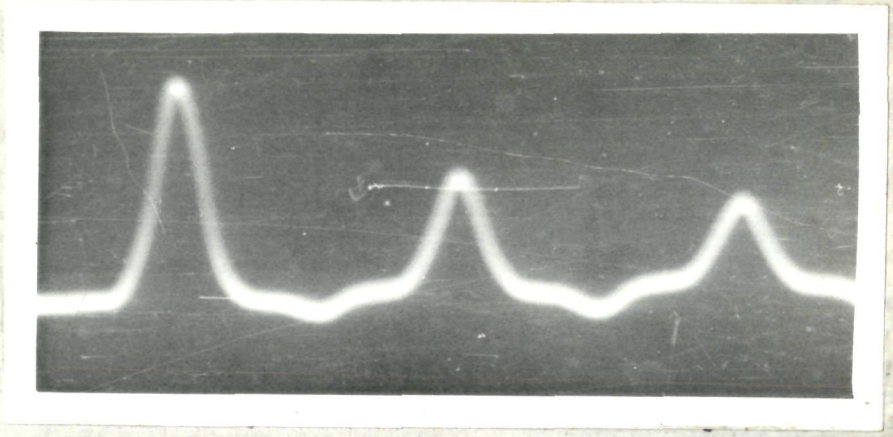
[D] Switching Angle $\partial = 120^{\circ}$

[E] Switching Angle $\partial = 150^{\circ}$

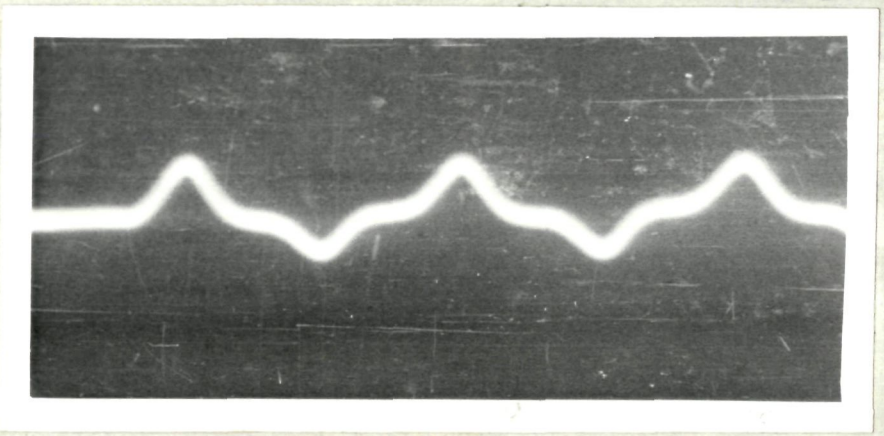
[F] Switching Angle $\partial = 180^{\circ}$



[A]



[B]



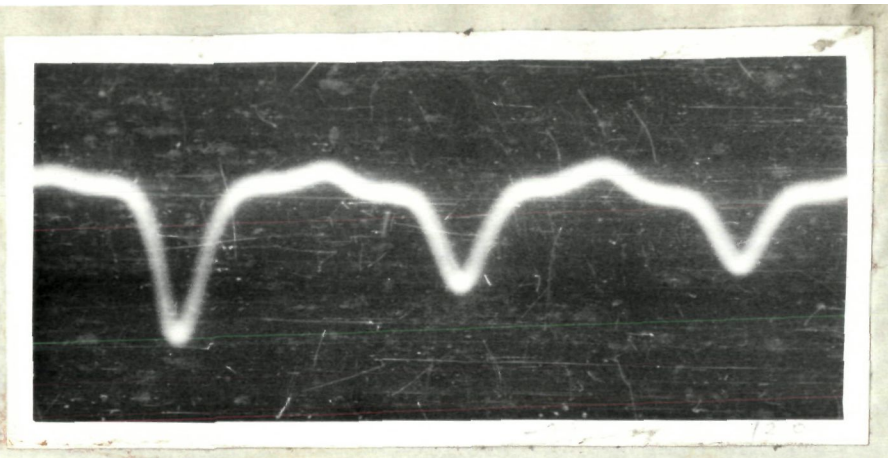
[C]

Fig. 5.3 Switching Transients in Transformer

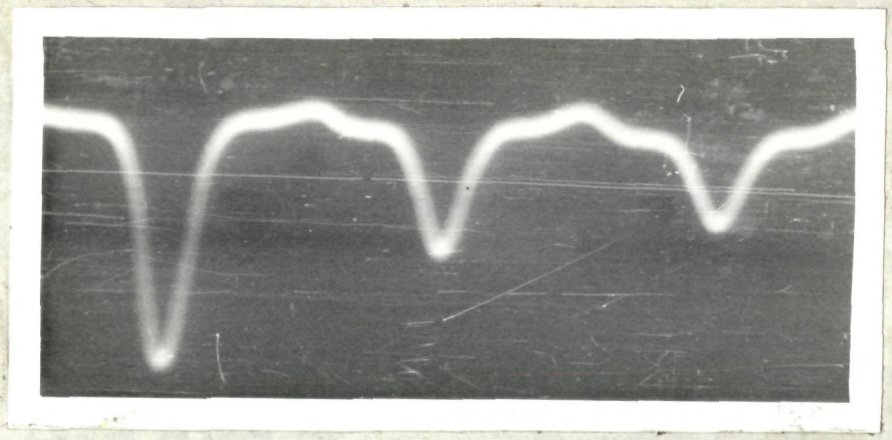
[A] Switching Angle δ = 30°

[B] Switching Angle δ = 60°

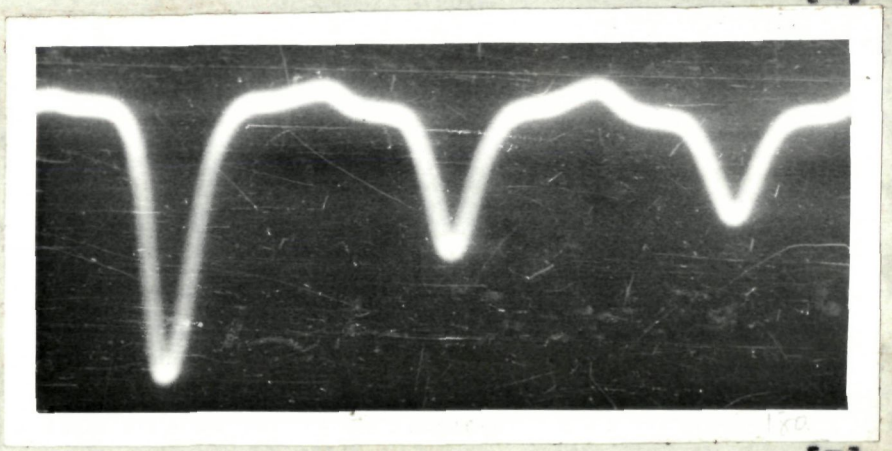
[C] Switching Angle δ = 90°



[D]



[E]



[F]

Fig. 5.3 Switching Transients in Transformer

[D] Switching Angle δ = 120°

[E] Switching Angle δ = 150°

[F] Switching Angle δ = 180°

The experimental results are plotted alongwith the estimated results. It is seen that the two are quite in confirmity with each other.

As estimated, no transients are present in the inrush current if switching-on takes place at the peak value of the voltage. A deviation from the above, enhances the transients.

CHAPTER - 6

C O N C L U S I O N

CONCLUSION

A complete controlled instant switching scheme is designed, fabricated and tested in the Lab. The usefulness of the controlled instant switching is demonstrated by studying the value of inrush current at various switching instants for a transformer availeble in the Lab. Switching delay is controlled by counting the number of pulses of an standard H.F. Generator and not by R.C. delay circuit, hence the control is more reliable and accurate as compared to schemes which use R.C. delay circuits. Also the operation is independent of variations in supply voltage and unaffected by noise and stray pulses as no monoshot is used in the circuit.

The scheme can be extended to 3-ϕ-controlled instant switching which will be suitable for 3-ϕ transformer. Also the frequency of H.F. Generator can be increased to obtain more accuracy. With suitable modification in the combinational logic, the number of settings can also be increased.

APPENDICES

```
100           DIMENSION C1(400),CMG(70),PHG(70)
200           LMAX=70
300           READ(8,88) EM,OMEGA,R1,R2,AL2,DT,AN1,AN2,(PHG(I),I=1,70),(CMG(I),
400          6I=1,70)
500     88    FORMAT(8F10.4/(10F8.6))
600             DELTD=-30.0
700             DO 20 N=1,7
800             DELTD=DELTD+30.0
900             DELTA=DELTD*0.01746
1000            WRITE(5,27) DELTD
1100    27      FORMAT(/1X,120('*')//40X,'DELTA = ',F6.1//1X,120('*')/)
1200            C2=0.0
1300            PHI=0.0
1400            I=0
1500            T=0.0005
1600            C1(1)=0.0
1700    50      I=I+1
1800            IF(I.EQ.1) GO TO 7
1900            IF(I.GT.400) GO TO 60
2000            L=2
2100    4       LL=L-1
2200            IF(PHI.GE.0.0) GO TO 2
2300            PHI=ABS(PHI)
2400            NEG=1
2500    2       IF(PHI-PHG(L)) 1,3,3
2600    3       L=L+1
2700            IF(L.EQ.LMAX) GO TO 1
2800            GO TO 4
2900    1       CMC=CMG(LL)+(CMG(L)-CMG(LL))/(PHG(L)-PHG(LL))*(PHI-PHG(LL))
3000            IF(NEG.EQ.0) GO TO 6
3100            CMC=-CMC
3200            NEG=0
3300            PHI=-PHI
3400    6       C1(I)=CMC+AN2/AN1*C2
3500    7       DPHI=(EM*SIN(OMEGA*T+DELTA)-R1*C1(I))*DT/AN1
3600            DC2=0.0
3700            C2=C2+DC2
3800    22      T=T+DT
3900            PHI=PHI+DPHI
4000    55      FORMAT(1X,4(10F10.4/))
4100            GO TO 50
4200    60      WRITE(5,55) (C1(I),I=1,400)
4300    20      CONTINUE
4400            END
```

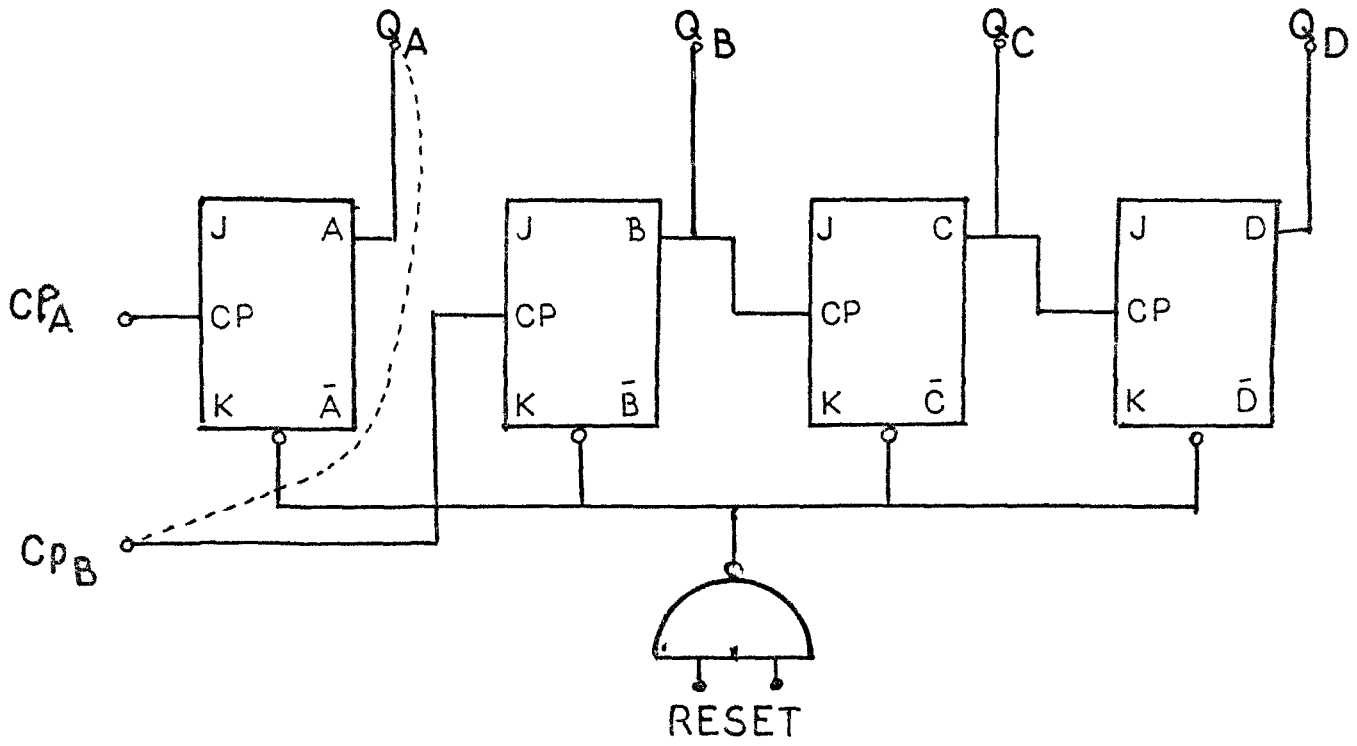
Appendix [A]

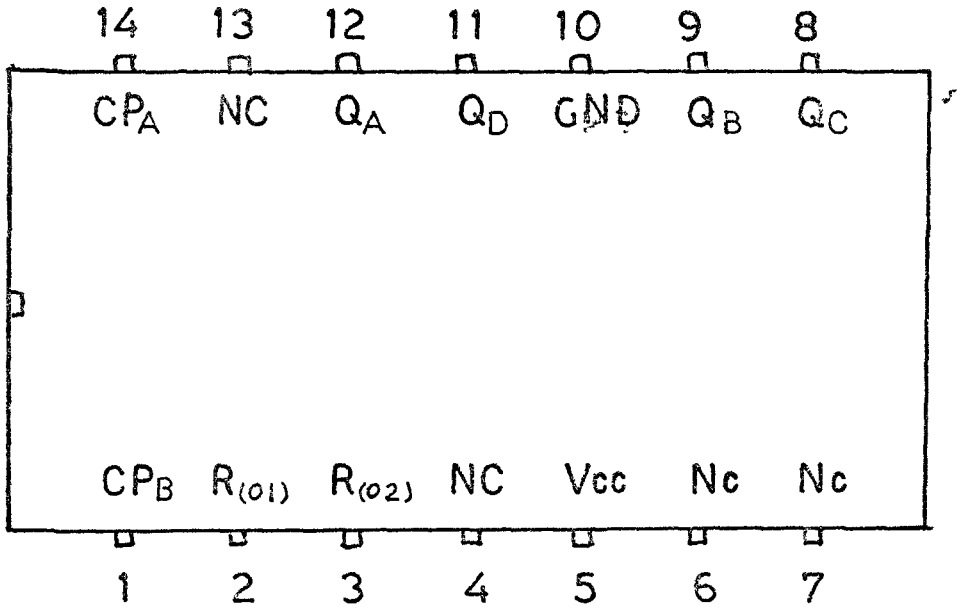
[Computer program for computation of primary current while secondary side open circuited]

```
100           DIMENSION C1(400),CMG(70),PHG(70)
200           LMAX=70
300           READ(8,88) EM,OMEGA,R1,R2,AL2,DT,AN1,AN2,(PHG(I),I=1,70),(CMG(I),
400          6I=1,70)
500     88    FORMAT(8F10.4/(10F8.6))
600              DELTD=-30.0
700              DO 20 N=1,7
800              DELTD=DELTD+30.0
900              DELTA=DELTD*0.01746
1000             WRITE(5,27) DELTD
1100    27       FORMAT(/1X,120('*')//40X,'DELTA = ',F6.1//1X,120('*')/)
1200             C2=0.0
1300             PHI=0.0
1400             I=0
1500             T=0.0005
1600             C1(1)=0.0
1700    50       I=I+1
1800             IF(I.EQ.1) GO TO 7
1900             IF(I.GT.400) GO TO 60
2000             L=2
2100    4        LL=L-1
2200             IF(PHI.GE.0.0) GO TO 2
2300             PHI=ABS(PHI)
2400             NEG=1
2500    2        IF(PHI-PHG(L)) 1,3,3
2600    3        L=L+1
2700             IF(L.EQ.LMAX) GO TO 1
2800             GO TO 4
2900    1        CMC=CMG(LL)+(CMG(L)-CMG(LL))/(PHG(L)-PHG(LL))*(PHI-PHG(LL))
3000             IF(NEG.EQ.0) GO TO 6
3100             CMC=-CMC
3200             NEG=0
3300             PHI=-PHI
3400    6        C1(I)=CMC+AN2/AN1*C2
3500    7        DPHI=(EM*SIN(OMEGA*T+DELTA)-R1*C1(I))*DT/AN1
3600             DC2=(AN2*DPHI-R2*C2*DT)/AL2
3700             C2=C2+DC2
3800    22       T=T+DT
3900             PHI=PHI+DPHI
4000    55       FORMAT(1X,4(10F10.4/))
4100             GO TO 50
4200    60       WRITE(5,55) (C1(I),I=1,400)
4300    20       CONTINUE
4400             END
```

APPENDIX(A)

[Computer program for computation of primary current for full load at secondary side]





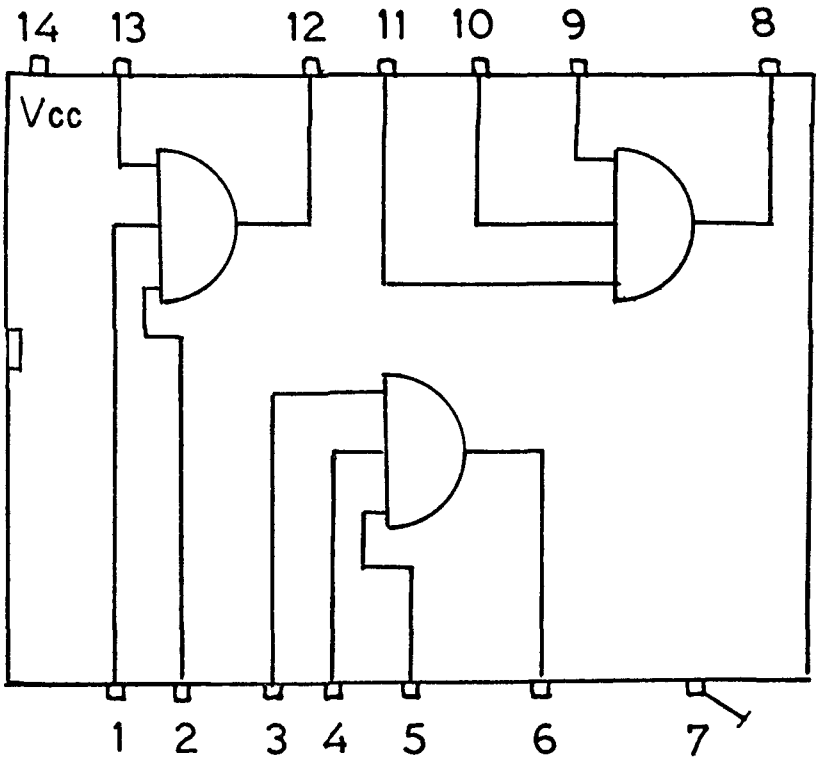
PIN DIAGRAM OF COUNTER 7493

Instructions :

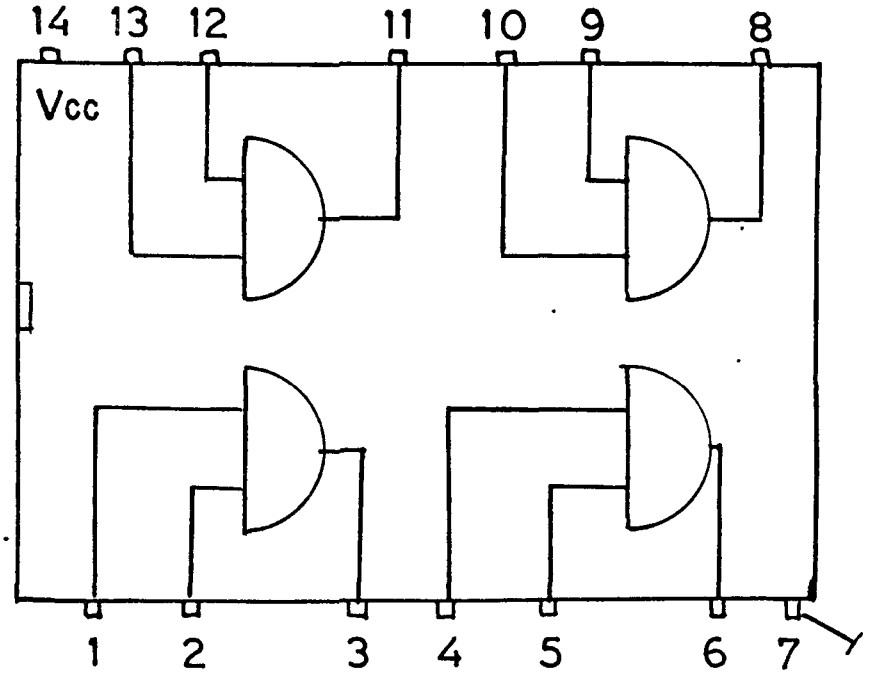
No.1. Output Q_A connected to output CP_B.

No.2. To reset all outputs to low level with $R_{O(1)}$ and $R_{O(2)}$ inputs must be at high level states.

No.3. Either (or both) reset inputs $R_{O(1)}$ and $R_{O(2)}$ must be at a low level to count.

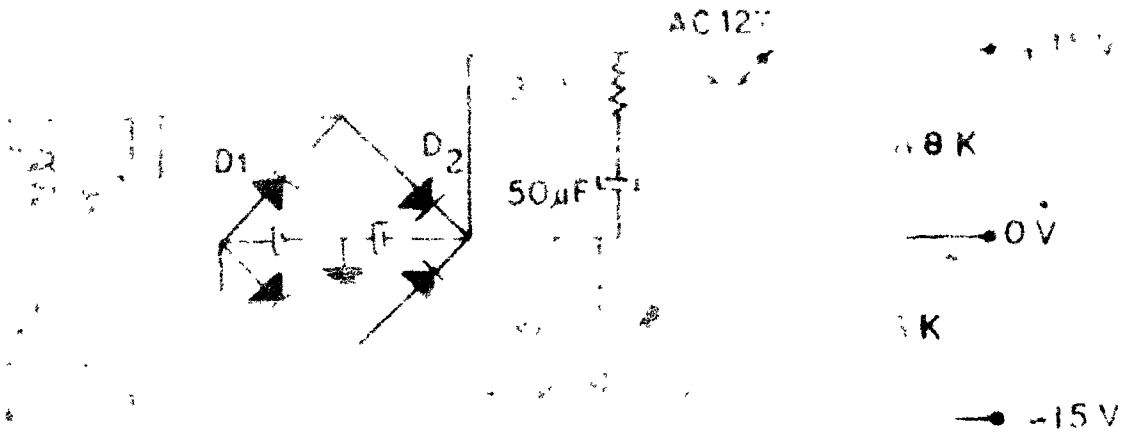


PIN DIAGRAM OF 3-INPUT AND GATE 7411

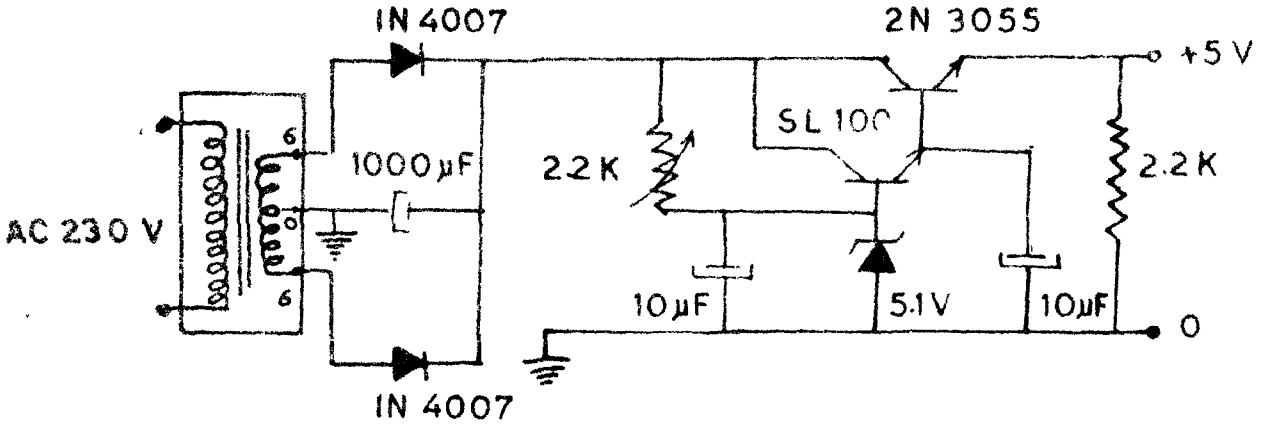


PIN DIAGRAM OF QUARD 2-INPUT AND GATE 7408

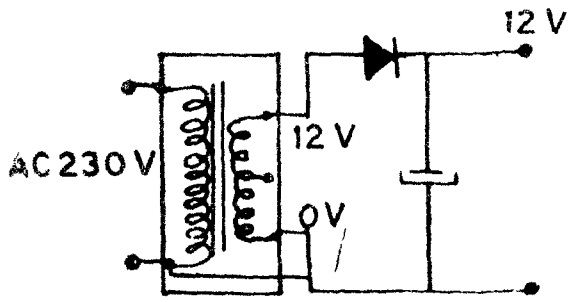
Appendix [D]



(A) ± 15 VOLT SUPPLY

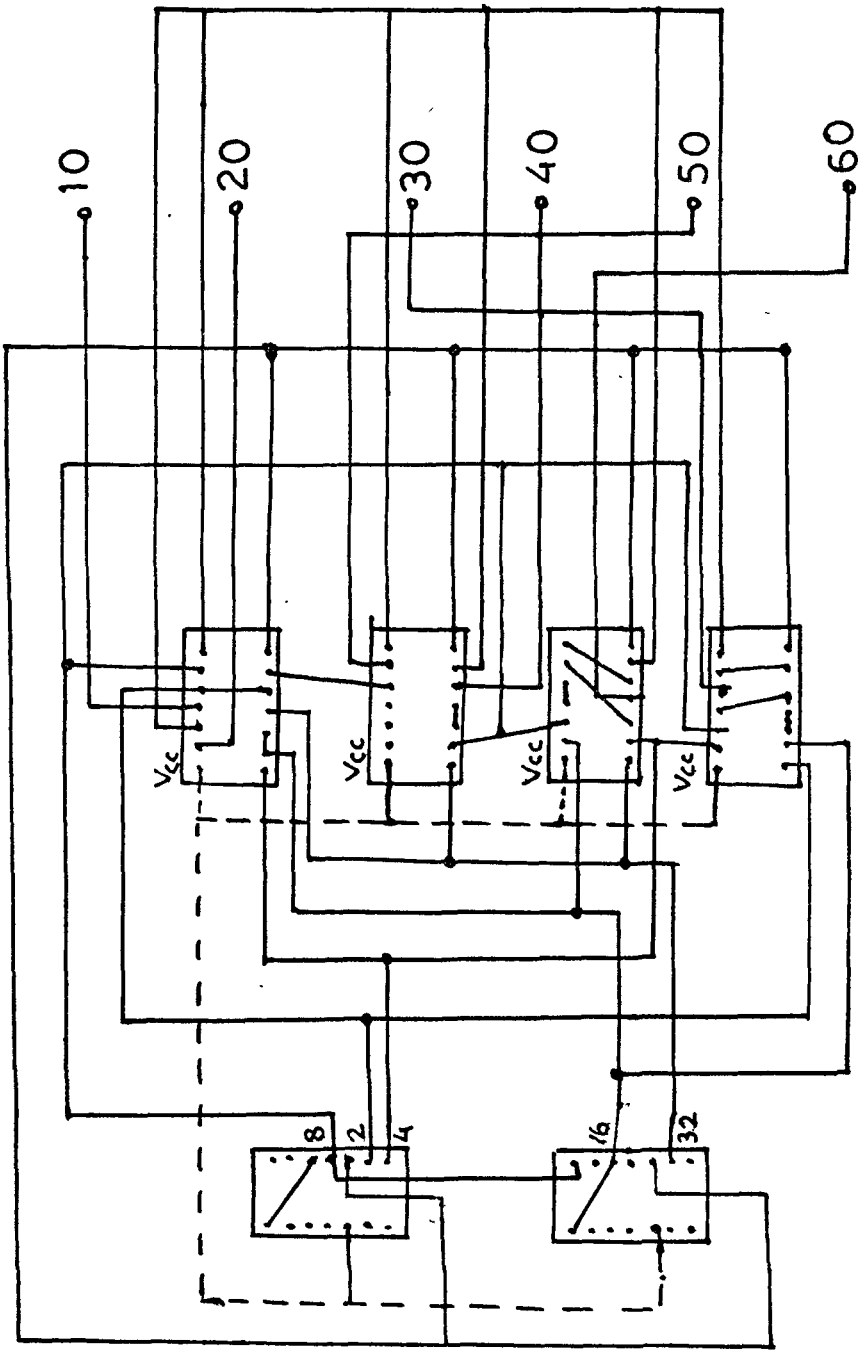


(B) + 5 VOLT SUPPLY



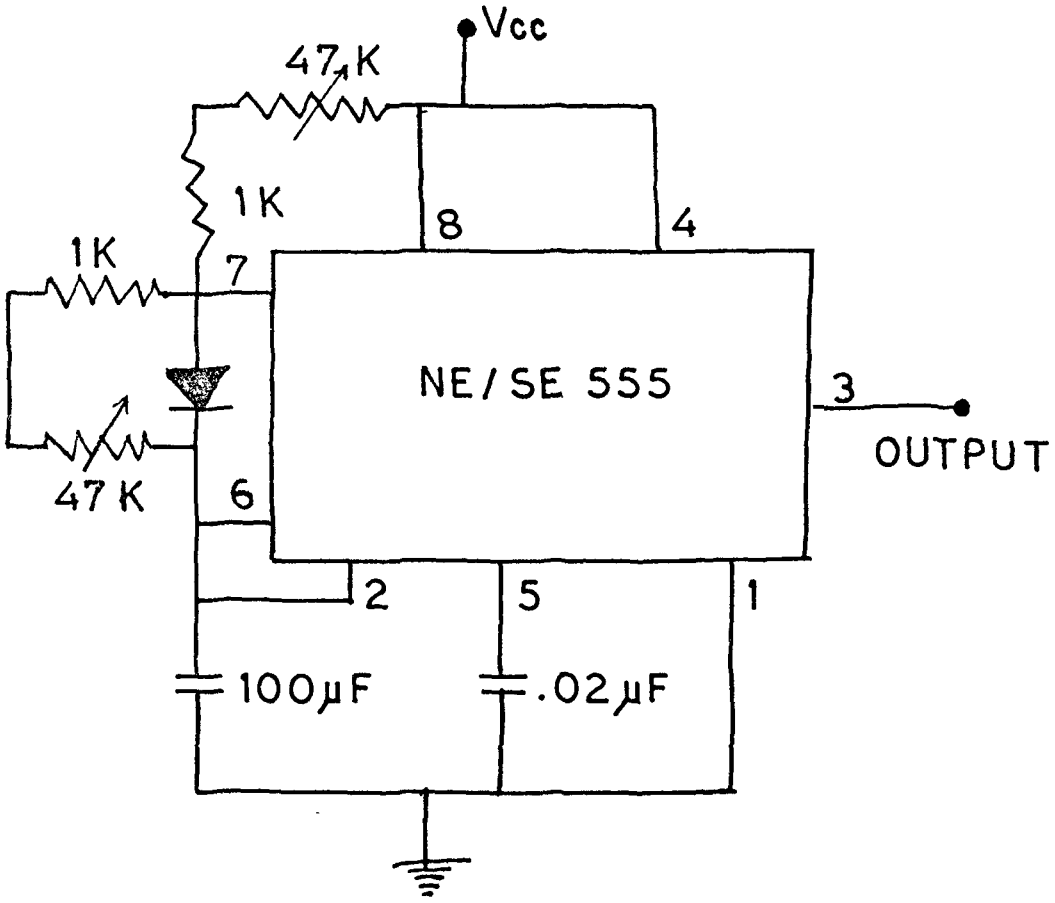
(C) 12 VOLT SUPPLY

POWER SUPPLIES



LAY OUT DIAGRAM OF CARD (A)

Appendix [E]



LOW FREQUENCY PULSE GENERATOR

REFERENCES

REFERENCES

1. K.M. Kerchner and G.F. Corcorn, 'Alternating Current Circuits' Chapter-XIV, POPPAN Printing Co.

2. Soni, Gupta and Bhatnagar, 'A Course in Electrical Power' Part-II, Chapter-3, DHANPAT PAI and SONS.

3. A.C. Monteith, C.F. Wagner, 'Electrical Transmission and Distribution', Chapter-5, Reference Book, OXFORD and IBH.

4. M.G. Say, 'The Performance and Design of AC Machines', Chapter-5, SIR ISAAC PITMAN and SONS.

5. L.F. Kennedy and C.D. Hayward, 'Harmonic Current Restraint Relay for Differential Protections', Trans. I.E.E.E., Vol. 57, May 1938, page 262-277.

6. E.P. Dick, W. Watsov, 'Transformer Model for Transients Studies Based on Field Measurement', I.E.E.E. Transaction Power Appar. and Syst. (SAA) Vol. PAS-100, No. 1, page 409-49, June-1981.

7. R. Yacamine, A. Abu Nasser, 'Numerical Calculation of inrush Current in Single Phase Transformer', Deppt. of Electrical Engineering and Electronics, University of Manchester, England, I.E.E. Proc. B (GB), Vol. 128, No. 6, page 327-34 (Nov.-81).

8. Jacob Millman and Christos C. Halkias, 'Electronic Devices and Circuits', Chapter-17, McGraw Hill KOGA-KUSHA.

9. R.M.M. OBERMAN, 'Electronic Counter', Chapter-3, Macmillan.

10. F.E. Gentry and F.W. Gulrwiller, 'Semiconductor Controlled Rectifiers', Chapter-2 and 4, PRENTICE-HALL.

11. Semi Conductors Limited, 'Regd. Office-Radio House', 6K, Dubash Marg, Bombay-400001.

12. Millman and Taub, 'Pulse and Digital Circuits', Chapter-II, McGRAW-HILL.